COMMONWEALTH OF AUSTRALIA

DEPARTMENT OF NATIONAL DEVELOPMENT

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS

RECORD No. 1968 / 32

Crystal Timing Unit Type NCD 2

by

M.S. JONES

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C O N T E N T S

ILLUSTRATIONS

SUMMARY

The Crystal Timing Unit type NCD2 is a fully transistorised crystal-controlled clock designed in 1964 for use at seismological field stations in the Territory of Papua & New Guinea in the crustal thickness project. It has an accuracy of better than three seconds per month and provides time marks to seismic recordings or to operate external timing systems. A comparison can be made with standard radio time-signals, and the difference between the unit's time and radio time, to an accuracy of ± 10 milliseconds, is displayed on the unit and can be corrected. Also included in the unit is a power amplifier capable of providing a frequency-stable 50-c/s, 240-volt, 30-watt power source for the operation of external equipment. The unit can be operated from any suitable 11 to 16 volts, 6 amp, d.c. input.

1. SPECIFICATIONS

Input power requirements:		11 to 16 volts, 6 amps d.c.
Power output available:		240 volts r.m.s. 50 c/s 30 watts a.c.
Crystal:	Fundamental frequency:	100 Kc/s ± 0.003%
	Type:	Pye +5° X-cut, temperature controlled
	Oven temperature:	75°C ± 2°C
	Thermostat control:	± 0.1°C
Timing accuracy:		Adjustable to better than 1 part in 10^6
Correction facilities:		Mechanical and electronic
Relay operations:		MAKE and BREAK contacts operating each second for 30 milliseconds. MAKE contacts operating each minute from 00 to 02 seconds with omissions each sixth hour. MAKE contacts operating each hour from 00 to 04 seconds with omissions each sixth hour.
Finish:		Black anodised with white-filled engraving.
Dimensions:		14½in x 16in x 8 in
Packing weight:		46 lb

2. GENERAL DESCRIPTION

2.1 Introduction

The Crystal Timing Unit type NCD2 is basically a crystal-controlled clock, which was designed and developed by the Design and Development Group of the Bureau of Mineral Resources to meet the special requirements for use at seismological field stations in the Territory of Papua & New Guinea in the crustal thickness project. The first completed unit was sent to Port Moresby in September 1964 and a total of four units have been built and have operated satisfactorily. Most of the design and development was done by I.P. Macfarlane until his resignation from the BMR, when the work was completed by K.J. Seers. The mechanical clock was designed by W. Olbrich.

It provides a time display and relay operations at predetermined intervals of time with a relatively high degree of accuracy. The precision-timed relay contacts can be connected to apply time-marks to seismic recordings, or can be used to operate external timing systems, to suit specific requirements.

Included in the unit is a power amplifier capable of delivering 30 watts at 50-c/s and 240-volts a.c. to external loads. As the frequency is derived from the crystal oscillator any frequency-dependent device such as a synchronous motor can be operated with the same order of timing accuracy.

Provision is made for comparison with standard radio time-signals and for errors to be corrected. A readout of the difference between the unit's time and radio time, to an accuracy of $\pm$ 10 milliseconds, is displayed on the front panel of the unit (see Plate 1).

Monitoring indicators, time display dials, reset and clock correction facilities, and all connector sockets, are also located on the front panel.

The unit is fully transistorised. It can be operated from any suitable 11 to 16 volts d.c. input source. When the 240-volt power amplifier is fully loaded, the input current required is approximately 6 amps.

Overload circuits, d.c. fusing, and a reverse-polarity relay circuit ensures that the unit is adequately protected in the event of component failures or incorrect d.c. input connections.

Circuit designs and components have been carefully selected for long-term stability and reliability. Square (or rectangular) wave forms have been used wherever possible to maintain constant times between triggering pulses.

Plug-in type circuit cards have been used extensively. This simplifies field servicing and permits the unit to be adapted, with a minimum of modification, for other applications that require accurate timing.

2.2. Functions

The functions of the Crystal Timing Unit are:

(1) To provide a measurement and display of time with an accuracy of better than 1 part in 10^6 (i.e. less than 3 seconds per month).

(2) To use this measurement of time to operate relays each second, minute, and hour, except where omissions are required (see Section 1 - Specifications).

(3) To provide a frequency-stable 50-c/s 240-volt power source for the operation of external equipment.

2.3. System concept (Plate 2)

The Crystal Oscillator Unit (01) generates a stable 100-Kc/s signal, which is connected, via the Sync. Comparator Unit (SA1), to two identical Decade Frequency Divider Units (DV1/1 and DV1/2). The frequency division ratio is normally 1000:1, producing a 100-pps output from each divider. The ratio can be altered to 900:1 or 1100:1 by means of the ADVANCE or RETARD microswitches on the front panel, which increase or decrease the output frequency accordingly. This advances or retards clock time and enables corrections to be made.

The function of DV1/2 is to check the operation of DV1/1. Outputs of 100 pulses per second from both units are connected to a comparison circuit in the SA1 unit. If the units are synchronised the SYNCH neon indicator on the front panel is struck by the pulses at the rate of 100 times per second; if they are out of synchronisation, the indicator will only be struck by occasional coincidental pulses. Should the oscillator circuits fail, the indicator will glow continuously and appear brighter than normal.

To ensure that the dividers are synchronised after time corrections have been made, the signal from the oscillator is blocked for 14 milliseconds whenever either the ADVANCE or RETARD switch is released after operation. During this period any dividing cycle in progress in the dividers is completed and the circuits relax to their stable states. Both units can then be simultaneously triggered when the oscillator signal is restored.

The output from DV1/1 is connected to two Bistable Frequency Divider Units (DV3/1, DV3/2) and to a Time Comparator Unit (SA4).

DV3/1 and DV3/2 are identical biscale dividers which produce 50-c/s square-wave outputs from their common 100 pps inputs.

The output from DV3/1 is amplified in the Power Amplifier Unit AM1 to provide the voltage required to drive the synchronous clock-motor on the Time Display Unit (TD1) at the constant speed of 1 revolution per second. A sine-wave drive for the clock motor is obtained by a low-pass

filter in TD1.

The clock-motor is mechanically coupled to a reduction gear-train which has output shafts engineered to revolve once each second, minute, hour, and 24 hours. Hands attached to the output shafts sweep over engraved dials, providing a display of time. On the same shafts, behind the dials, are slotted discs which are interposed between photo-transistors and their operating light sources. When a disc rotates to a position that allows light to fall on to a photo-transistor, a monostable multivibrator associated with that photo-transistor is triggered (via gating circuits) and a relay is operated precisely at the time required by the NCD2 specifications.

So that the time interval between individual relay operations is not affected by minor variations such as changes in photo-transistor triggering conditions, mechanical backlash in the gear-train, etc., a 50-c/s square-wave signal from DV3/2 gates the commencement of each relay operation.

The output from DV3/2 is amplified, first by Power Amplifier Unit AM2, and then by the main Power Amplifier, AM3, to produce a 30-watt, 240-volt r.m.s., 50-c/s power source for the operation of external equipment.

Time comparisons with standard radio time-signals for errors of less than 1 second are made by pulse gating and counting circuits.

A RESET switch on the front panel prepares the comparison circuits. Pulses from the output of DV1/1 (which are normally blocked) are gated through the Time comparator Unit (SA4) for the differences in time between the incidence of a 1-second relay pulse and a 1-second radio signal. Gating can be commenced by either a relay pulse or a radio pulse according to the position of the FAST-SLOW switch on the front panel. If gating is started by a relay pulse it is stopped by a radio pulse and vice versa.

The pulses gated through SA4 are connected to the input of the Decade Divider and Readout Unit DV2/1. This unit transmits one output pulse for each ten input pulses to a similar unit, DV2/2. In both units the pulses are counted and converted to currents which are directly proportional to the number of pulses appearing at their inputs. As the pulses are exactly one-hundredth of a second apart the currents which are read on readout meters on the front panel indicate clock error to this accuracy.

For errors of 1 second or more, the position of the 1-r.p.m. hand on the SECOND dial is observed when a 1-minute radio signal is heard. From this observation and the readings on the readout meters an accurate time comparison, to the nearest ± 10 milliseconds, can be made.

The Voltage Regulator Units PP1, PP2, and PP3 provide the -6V, -9V, and -10V regulated d.c. supplies required by the NCD2 units. Each regulator incorporates a cut-out circuit, which operates automatically if currents or voltages exceed predetermined limits.

A -90V Generator Unit PP4 provides the voltage required for operating the various neon indicators used in the Timing Unit.

The operation of the power supplies and the synchronisation condition is indicated by lamps mounted on the front panel of the NCD2.

3. CIRCUIT DESCRIPTIONS

3.1 Crystal Oscillator Unit 01 (Plate 3)

The Crystal Oscillator Unit 01 consists of a 100-kc/s crystal oscillator and clipper and amplifier circuits. The complete unit is mounted on a plug-in circuit card, with the exception of the quartz crystal, which is mounted on the main NCD2 chassis in a thermostatically controlled oven. The oscillator unit is operated from a regulated -6volts d.c. supply but the oven heater winding is connected to the unregulated 11 to 16 volts d.c. input source.

A $+5^{\circ}$ X-cut crystal operates between its natural parallel and series modes; its reactance therefore is inductive. This inductance, in conjunction with C1, C2, and C6 form a resonant circuit at the fundamental frequency of 100Kc/s. C2 is a trimmer capacitor which can adjust the frequency to compensate for small component differences, long-term crystal drift, etc.

A positive feedback path between the collector and base of Q1 maintains oscillation. An AGC voltage is applied to the base of Q1. Under normal operating conditions this limits the drive to the crystal and keeps the output amplitude constant. It also allows the circuit to operate at maximum gain when starting up. The output from the collector of Q1 is taken, via C3, to the base of Q2.

Q2 is a conventional common-emitter amplifier. Output signals from its collector are (1) used to develop the AGC voltage, and (2) to provide the drive voltage for subsequent circuits.

(1) An output voltage from Q2 is applied through R6 and C11 to the junction of diodes CR1 and CR2. CR1 and CR2 form a voltage doubler circuit which charges C10. The voltage developed across C10 is applied through R9 as an AGC voltage to the base of Q1. As CR1 and CR2 are silicon diodes the AGC does not become fully effective until the voltage exceeds approximately 1 volt. Hence the oscillator can commence to operate at maximum gain but the gain is reduced as the AGC voltage builds up.

(2) The other signal from the collector of Q2 is also applied to two silicon diodes CR3 and CR4 via R7 and C7. The two diodes form a clipping circuit. On the positive half-cycles when the signal exceeds approximately 0.5 volt CR3 becomes forward-biased and any further rise in potential is prevented by diode action. Similarly the negative half-cycles are limited by CR4. The resultant waveform is a 1-volt peak-to-peak square wave which has a fast rise-time (0.5 microsecond). Capacitors C7 and C8 isolate CR3 and CR4 from d.c. potentials and provide the signal coupling to the following circuit.

Q3 is another conventional common-emitter amplifier. The output from Q3 is coupled to Q4 through C4 and R8, a pulse-shaping network, to maintain the fast rise-time.

The signal applied to the base of Q4 is of a large enough amplitude to consider Q4 as a switching amplifier biased by CR5. R15 ensures that CR5 is forward-biased throughout the entire switching cycle.

The output from Q4 is a well-shaped 100-kc/s square wave, approximately 6 volts peak to peak, which is coupled, via the S.1 unit, to the Decade Frequency Divider Units DV1/1 and DV1/2 (see Plate 2).

3.2. Synchronisation Comparator Unit SA1 (Plate 4)

The Synchronisation Comparator Unit SA1 contains two separate circuits which perform the following functions:

(1) The output signals from Decade Frequency Divider Units DV1/1 and DV1/2 are compared and their synchronisation condition indicated by a neon indicator mounted on the

front panel of the NCD2.

(2) If the signals are not synchronised, facilities are provided to resynchronise them.

General Description of Operation. A simplified diagram (Figure 1) illustrates the operation of the unit.

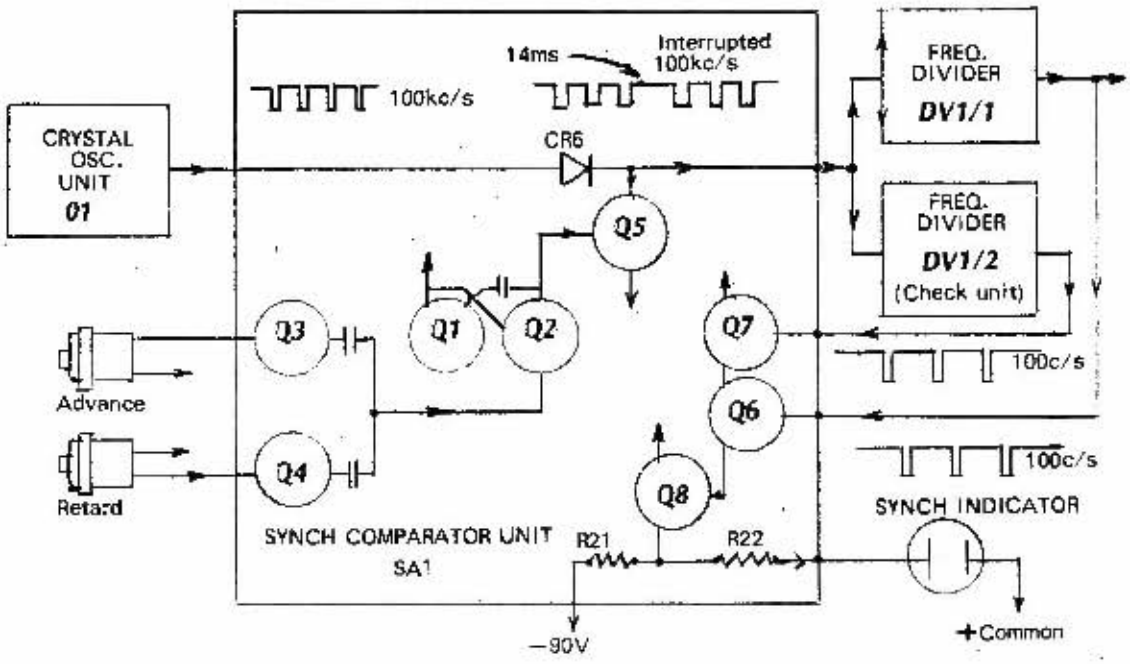


Figure 1

Under normal operating conditions the 100-Kc/s signal from the oscillator passes through CR6 to the input circuits of DV1/1 and DV1/2. The output signals from DV1/1 and DV1/2 are each 100 p.p.s. The DV1/1 output is connected to the base of Q6 - and also to the inputs of DV3/1, DV3/2, and SA4 (see Plate 2). The output from check unit DV1/2 is connected to the base of Q7. Q6 and Q7 are in a NAND gate circuit, which only passes current when simultaneous negative pulses are applied to both bases.

The collector of Q6 is connected to the base of Q8 so that when Q6 and Q7 are conducting, Q8 is cut off. The collector of Q8 is at -90 volts under these conditions because of the negligible voltage drop across R21. As the SYNCH neon indicator is also connected to the Q8 collector, via R22, it will be struck.

When Q6 and Q7 are not conducting, Q8 is switched on, the potential at the collector is reduced to a few volts by the drop across

R21, and the neon indicator is off.

If the outputs from DV1/1 and DV1/2 are synchronised the SYNCH indicator will be operated 100 times per second, which appears as a continuous glow. If the divider units are not synchronised the indicator will strike only when occasional pulses coincide. If the oscillator circuit fails, Q8 is switched off and the indicator glows with an intensity brighter than normal.

When it is required to restore synchronisation a momentary operation of either the ADVANCE or RETARD switch produces in either Q3 or Q4 a trigger pulse to operate a monostable multivibrator (Q1 and Q2). The output from the monostable multivibrator switches Q5 on and Q5 blocks the oscillator signal from the divider units for the 14-millisecond quasi-stable period of the monostable multivibrator. The divider circuits relax to a stable condition and both units are triggered simultaneously by the first signal pulse after the interruption. Provided that their frequency-division ratios are identical, DV1/1 and DV1/2 outputs will then be synchronised.

As a trigger pulse for the monostable multivibrator (Q1 and Q2) is initiated by the release of either the ADVANCE or RETARD switch the dividers are synchronised automatically when clock corrections are made.

Detailed Description of Operation. With reference to Plate 4 Q1 and Q2 are in a monostable multivibrator circuit (see Appendix 1) which can be triggered by a positive pulse from either Q3 via C2 or from Q4 via C3. The quasi-stable period of the monostable multivibrator is determined by the time constant of C1 and R2. Diode CR3 and R3 have been incorporated to isolate the collector of Q2 from C1 when the monostable multivibrator, having been triggered, is returning to a stable condition. While C1 is recovering from discharge, CR3 is reverse-biased. Therefore since Q2 is cut off, its collector can rapidly go to -6 volts without being affected by the potential on C1, which is charging through R3. Consequently the fall-time of the monostable multivibrator output pulse is very rapid, which allows the Q5 circuit to which it is connected to be cut off sharply.

The collector of Q2 is connected to the base of Q5. Q5 is normally cut off but it conducts for the quasi-stable period of the monostable multivibrator. The emitter of Q5 is connected to the diode CR6, which is in the 100-Kc/s signal line. When Q5 conducts, CR6 is reverse-biased, the 100-Kc/s signal is blocked, and the divider circuits relax to their stable condition. The synchronisation is restored when the

oscillator signal is again applied to the divider unit inputs.

Positive-going voltages to trigger the monostable multivibrator are originated as follows:

Q3 is normally-biased by voltage divider R14-R15. R14 is connected to the -6 volt supply through the normally-made contacts of the ADVANCE switch. When this switch is operated the supply is disconnected, Q3 is cut off, and its collector goes to -6 volts. When the switch is released, Q3 again conducts, the collector goes positive, and the positive change through C2 triggers the monostable multivibrator.

Q4 is an NPN transistor, connected as an emitter-follower, which is normally forward-biased by R16. When the RETARD switch is operated, -6 volts is applied, via the switch contacts, to the base of Q4, cutting Q4 off, and the emitter potential goes to approximately -5.5 volts. When the RETARD switch is released, Q4 conducts, the emitter goes positive, and the monostable multivibrator is triggered via C3.

Q6 and Q7 are connected in a NAND gate circuit (see Appendix 3) i.e. two simultaneous negative pulses are required to produce a positive output pulse. Under normal operating conditions the circuit will gate the pulses only if the negative outputs from DV1/1 and DV1/2, applied to the bases of Q6 and Q7, are coincidental.

The collector of Q6 is connected to the base of Q8. The Q8 emitter is held by zener diode CR9 at -4.7 volts. Its collector is connected to the junction of R21 and R22. -90 volts is applied to R21, and R22 is connected to an NE51 neon SYNCH indicator on the front panel, the other side of which goes to positive COMMON.

During the non-conducting periods of Q6 and Q7, Q8 is forward-biased, and the current through Q8 drops the -90 volts across R21 to a few volts. As this is the potential applied to the NE51 through R22 the neon will not operate.

When the NAND gate conducts, Q8 is cut off, the potential at the collector, and therefore applied to the NE51, is -90 volts, and the indicator glows.

The SYNCH indicator, then, monitors the state of synchronisation of the two Frequency Divider Units (DV1/1 and DV1/2).

3.3. Decade Frequency Divider Units DV1/1 and DV1/2 (Plate 5)

The Decade Frequency Divider Units DV1/1 and DV1/2 are identical and interchangeable. Each unit consists of a cascade of three monostable multivibrators which reduces the 100-Kc/s signal from the oscillator in decade steps to 10-Kc/s, 1-Kc/s, and finally to 100 p.p.s. The sole function of DV1/2 is to provide a check on the operation of DV1/1.

The 100-Kc/s square-wave signal from the Oscillator Unit (01), via the Synchroniser Comparator Unit (SA1), is applied to the emitter of Q2 through C4. Q1 and Q2 operate in a monostable multivibrator circuit (see Appendix 1) with a quasi-stable period that can be adjusted by R18 so that the monostable multivibrator is triggered by every 10th input pulse. The output of 10-Kc/s is taken from the collector of Q2 through a conventional emitter-follower, Q3, to reduce the capacitive loading on the collector of Q2 and so decrease the monostable pulse fall-time. This is applied to the emitter of the second monostable triggering transistor, Q5.

Q4 and Q5 form a circuit similar to that of the first monostable circuit except for the component values of the time-constant capacitor and resistors. The quasi-stable period of Q4 and Q5 is adjusted by R19 for an output frequency of 1-Kc/s.

The final monostable circuit, Q6 and Q7, normally divides the 1-Kc/s output from Q5 to 100 p.p.s. However, the frequency-division ratio can be altered from 10:1 to either 9:1 or 11:1 by the ADVANCE and RETARD switches on the front panel thereby increasing or decreasing the output frequency (and consequently the rate of the clock-motor in TD1) during clock corrections.

Whilst the ADVANCE and RETARD switches are in their normal positions -6 volts is applied through the normally-made contacts of the RETARD switch and CR5 to the junction of R11 and R12. This, in effect, shunts R11. When the RETARD switch is operated the shunt is removed and the time-constant governing the quasi-stable period of the monostable multivibrator is increased owing to the additional resistance of R11. Because of this the monostable circuit is still in its quasi-stable state when the 10th input pulse is applied but has resumed a stable condition before the application of the 11th pulse. Hence the frequency-division ratio is altered to 11:1, and the output frequency reduced to 90.9 p.ps. while the RETARD switch is held in.

When the ADVANCE switch is operated, -6 volts is applied through its normally-open contacts, via CR4 and R20, to the junction of R12 and R13. This effectively shunts R11 and R12; decreases the quasi-stable period; and changes the frequency-division ratio to 9:1, and the output frequency to 111.1 p.p.s. while the ADVANCE switch is held in.

With this facility the rate of the clock-motor can be altered as required to make corrections to clock time.

The output from Q7 is coupled to the load through another emitter-follower, Q8. No emitter-follower circuit has been included between the second and third monostables, as it is not essential at the lower frequencies for optimum performance.

3.4. Bistable Frequency Divider Units DV3/1 and DV3/2 (Plate 6)

The Bistable Frequency Divider Units DV3/1 and DV3/2 are identical units which each give a 50-c/s square-wave output from the common 100-p.p.s. input from DV1/1. Each unit consists of a bistable multivibrator, emitter-followers, and a push-pull pre-amplifier stage.

Q1 and Q2 are connected in a bistable multivibrator circuit (see Appendix 2), which, at any given instant, has one transistor conducting and the other cut off. This condition biases diodes CR3 and CR4 so that the first positive pulse applied to both C4 and C5 will be steered to the base of the conducting transistor. This cuts the conducting transistor off and reverses the bias conditions of CR3 and CR4. The resultant outputs from the collectors of Q1 and Q2 are square-waves, 180° out of phase, which are one-half of the frequency of the input pulses.

The 50-c/s square-wave outputs are applied to the bases of emitter-followers, Q7 and Q8. The outputs from the emitter-followers are capacitively coupled to the bases of Q3 and Q5, so that in the event of a failure of drive voltage the power amplifier transistors will be cut off thus being prevented from being damaged.

The pre-amplifier consists of two Darlington-connected common-emitter circuits, Q3 and Q4 and Q5 and Q6, in push-pull. In these circuits, Q4 and Q6 form the emitter load impedances for Q3 and Q5. The circuits have high input impedances which do not affect the coupling time-constants and therefore the waveforms of the bistable multivibrator.

Diodes CR7 and CR8 prevent false triggering of the bistable multivibrator by any voltage spikes developed on the square-waves.

The output voltage from DV3/1 drives Power Amplifier AM1. DV3/2 provides a relay-gating signal for the Light-gate Unit SA2 and the drive voltage for Power Amplifier AM2.

3.5. Time Comparator Unit SA4 (Plates 7 & 8)

The time error in the NCD2 can be ascertained by comparing clock time with standard radio time-signals. This is accomplished in two phases:

(1) By visual observation of the hands on the dials of the Time Display Unit (TD1) when a 1-minute time-signal is received. From this a comparison to within 1 second is obtained.

(2) By measurement of the interval between 1-second radio pulses and NCD2 1-second relay-drive pulses. This provides a comparison to one-hundredth of a second ($\pm$ 10 milliseconds).

From a combination of both, the clock error can be observed to the nearest one-hundredth of a second.

The function of the Time Comparator Unit, in conjunction with its associated circuits, is to perform the second part of this operation.

If there is any clock error - apart from whole seconds - there are two time intervals that can be measured:

(1) The interval (t_1 milliseconds) between the drive-pulse for the 1-second relay and the arrival of the next 1-second radio pulse, and

(2) The interval (t_2 milliseconds) between a radio pulse and the following relay-drive pulse.

Either interval can be measured, the selection being controlled by the position of the FAST-SLOW change-over switch on the front panel. It is therefore essential that the procedure outlined in Section 4 be strictly followed.

To measure interval t_1 the change-over switch applies a relay pulse to Q1 on the "Start" line and a radio time-signal pulse to Q3 via the "Stop" line. To measure interval t_2 the connections are reversed. Pulses from the output of DV1/1 are gated through SA4 to the input of DV2/1 for the interval of time selected by the change-over switch.

Q1 and Q2 and Q3 and Q4 are connected in two bistable multivibrator circuits (see Appendix 2). The emitters of Q1 and Q4 are biased by the -4.5 volts potential seen at the junction of R8 and R9. The emitters of Q2 and Q3 are connected to this bias through a pair of normally-made contacts of the RESET switch on the front panel. Before gating can be commenced the circuits must be cleared by operation of the RESET switch. This removes the bias from Q2 and Q3, therefore Q1 and Q4 become the conducting transistors in the bistable circuits. Q4 switches Q5 on, which in turn shorts out Q6.

A positive pulse on the "Start" line switches Q1 off, and Q2 conducts. The collector of Q2 is connected to the base of Q4 by C5 and CR3, so Q4 is then switched off. This turns Q5 off, removing the short form Q6. 100-p.p.s pulses from DV1/1 on the base of Q6 can now appear on the emitter, which is connected to the input of DV2/1.

Pulses from DV1/1 will continue to be gated through Q6 until a positive pulse on the "Stop" line switches Q3 off and Q4 and Q5 on, again applying a short on Q6.

Since the pulses from DV1/1 are one-hundredth of a second apart the number of pulses gated are a measure of the time interval t_1, or t_2, whichever has been selected by the FAST-SLOW change-over switch. The pulses are counted and displayed in subsequent circuits (see Section 3.9).

Q7 and Q8 are in a monostable circuit (see Appendix 1), which is triggered by radio-time signal pulses. The monostable output pulse is connected to the FAST-SLOW change-over switch, and to a trigger circuit in the PP4 unit, which operates a neon indicator on the Time Display Unit. The description and operations of these features are dealt with in their appropriate sections.

3.6. Power Amplifier Units AM1, AM2, and AM3 (Plates 9, 10, & 11)

The circuit details and principles of operation for each Power Amplifier Unit are basically the same, the main differences being the components selected to suit the requirements of each individual unit.

AM1 provides the 48-volt a.c. drive for the synchronous clock motor in the Time Display Unit (TD1).

AM2 provides the drive voltage required by AM3.

AM3 is the a.c. power amplifier. It is capable of a 30-watt output of 240 volts r.m.s. 50-c/s a.c. for delivery to external loads.

AM1 is operated from -9-volt Regulated Supply (PP2), and AM2 and AM3 from the -10-volt Regulated Suppy (PP3).

Each circuit consists essentially of two power transistors in a common-emitter, push-pull configuration, with transformer output loading.

In AM1 and AM2, silicon diode CR1, connected between the power transistor emitters and positive COMMON, ensures that the transistors are effectively cut off when positive half cycles are applied to their bases.

Two 3-watt, 1-ohm resistors, in series with the output leads of the AM2 transformer secondary winding, limit the base current of the AM3 power transistors.

A Voltage-Dependent Resistor (VDR), R1, is connected across the primary winding of each transformer to suppress voltage spikes. A further precaution in AM3 to prevent spikes from radiating is the inclusion of the 150-μF capacitor across the supply.

The VDR across the secondary on AM3 further reduces spikes from this unit and also prevents the output voltage rising excessively on no load.

A sensing line from the -10-volt Regulator Unit (PP3) to AM3 enables the regulating circuit to compensate for voltage changes that occur at the point of maximum current drain. Voltage changes due to drop through the resistance of the interconnecting wiring are thus taken into account.

3.7. Time Display Unit and Light-gate Generator TD1 (Plates 12 & 13)

The 48-volt 50-c/s square-wave from AM1 is passed through an LC filter, the sine-wave output of which is applied to the windings of a 250-r.p.s. synchronous motor with a 25:6 reduction gearbox. The 1-r.p.s. shaft of this gearbox is coupled to a reduction gear-train. Extending through the front and back plates of the gear-train are shafts that revolve at the rates of 1 r.p.s, 1 r.p.m, 1 r.p h. and 1 rev. per 24 hours.

Hands attached to the front extensions sweep over engraved dials providing the time display.

Each rear extension has a slotted disc fitted to it. Four small bracket assemblies which each hold an OCP71 photo-transistor and a miniature 6-volt lamp - selected for its long filament life rating - are mounted on the back-plate so that the discs are interposed between the OCP71s and their operating light sources. Light can only operate an OCP71 when the slot in a disc is in line with a lamp. The 24-hour disc has four slots, each 90° apart, and each other disc has a single slot, so that the OCP71s are operated each second, minute, hour, and six hours. The photo-transistor collectors are connected to their respective circuits in the SA2 unit. Negative temperature coefficient (n.t.c.) resistors are used in collector and base circuits to maintain stability of photo-transistor triggering through a wide range of temperature variations (see Plate 13).

When the NCD2 is first installed, or if a large correction to the clock is ever necessary, this can be made mechanically. A "one-way" clutch is fitted to the SECOND hand, which permits the hand to be moved rapidly in a clockwise direction using the detachable winder supplied. A special holder for the detachable winder is located in the bottom left-hand corner of the TD1 unit. For details of use see Section 4.

A small neon lamp mounted behind the MILLISECONDS dial is visible through a small aperture just below the "0" mark. It is operated once per second from radio time signals, via the SA4 unit, and is used to adjust the radio signal level for optimum operation of the DV2 readout units. It can also be used to check the position of the MILLISECONDS sweep hand relative to zero when the radio seconds signals occur.

3.3. Light-gate and monostable circuits, and timing relays, SA2 and SA3 (Plates 13, 14, & 15)

Design considerations made it impracticable to incorporate the entire time-marking system on the one plug-in unit. The system is comprised of:

(a) the photo-transistors and their light sources and the n.t.c. resistors in their base circuits, which are mounted on the TD1 Unit;

(b) The light-gate circuits and 1-second monostable circuit, mounted on the SA2 card; and

(c) the 1-minute and 1-hour monostable circuits, and the three timing relays on the SA3 card.

A block diagram of the complete time-marking system is presented in Plate 15. From this the sequence of operation can be seen as follows:

Gate A is a NAND gate;

Gates B, C, and D are AND gates (see Appendix 3).

A 50-c/s square-wave is applied continuously to gate D. The light-pulse from the 1-second photo-transistor is also applied to this gate. The light-pulse cannot trigger the 1-second monostable circuit until it coincides with the leading edge of a positive half-cycle of a.c., nor can the 50-c/s positive stops act as trigger pulses until the 1-second light pulse provides a gating condition.

Similarly the 1-minute monostable circuit is only triggered by an output from gate C when pulses from the 1-minute light-gate generator and the 1-second relay circuit coincide. Further it is essential for a pulse from the 1-minute relay circuit and the 1-hour light-gate generator to coincide to operate the 1-hour monostable circuit through gate B.

Consequently each relay closes, irrespective of minor variations of the light pulse triggering times, precisely at the beginning of a second.

The duration of each relay closure is determined by the time-constants of its associated monostable circuit.

The outputs from the 1-hour and 6-hour light-gate generators are applied to the NAND gate A. This provides an output pulse once every 6 hours, which is taken to gate C, preventing the operation of 1-minute and 1-hour relays. The resultant time-mark omissions provide identification of every sixth hour on seismic recordings.

Plate 13 is a circuit diagram of the SA2 Unit. The components shown within the dotted blocks are mounted on the TD1 Unit.

Considering firstly the 1-second circuit, the current through Q10 under normal (dark) conditions is negligible; therefore Q11 being forward-biased by R18 is conducting, the supply potential is dropped through R19, and the 50-c/s signals applied to the base of Q12 are ineffective.

A light-beam falling on Q10 through the slotted 1-r.p.s. disc in the Time Display Unit once each second causes a positive change to appear at the base of Q11 and a corresponding negative change at the Q11 collector.

As the monostable circuit Q13 and Q14 requires a positive trigger this change does not affect the monostable circuit. It does, however, apply the full supply potential across Q12, thus allowing the first positive half-cycle of a.c. on the base of Q12 to trigger the 1-second monostable circuit through C4.

In the 1-minute circuit, Q9 is conducting until a light pulse on Q8 cuts it off. While it is conducting, positive pulses from the 1-second relay circuit, via CR9 (Plate 14), are shunted by Q9. When Q9 is cut off the 1-second pulse occurring during the cut-off period triggers the 1-minute monostable circuit, Q4 and Q5.

In the 1-hour circuit, Q6 and Q7, normally forward-biased by R7 and R10 respectively, are cut off when Q5 is light-pulsed. Diodes CR4 and CR6 isolate the bases of Q6 and Q7 from each other, preventing any interaction. Q7 in SA2 and CR7 in SA3 operate in the same manner as Q9 in SA2 and CR9 in SA3 described above. This provides a trigger for the 1-hour monostable circuits from the 1-minute monostable circuit only when Q5 is light-pulsed.

Hourly negative pulses from the collector of Q6 are applied to the base of Q3. Six-hourly light-pulses from Q1 develop a negative pulse on the collector of Q2, which is applied to the base of Q4. Q3 and Q4 are connected in a NAND gate circuit, so a positive pulse appears on the collector of Q3 every 6 hours. This positive potential maintains CR3 forward-biased and consequently CR9 in SA3 is reverse-biased, thus the 1-minute monostable circuit cannot be triggered. With no 1-minute pulse to gate the 1-hour monostable circuit, neither relay operates under these conditions and the six hourly omissions are effected.

The 1-minute and 1-hour monostable circuits on the SA3 card (see Plate 14) are similar to the 1-minute circuit, the only difference being the component values governing the quasi-stable period of each circuit.

The emitter-follower and relay circuits are the same as the 1-second emitter-follower and relay.

A pulse developed across R15, through CR10, by the 1-second monostable circuit, is applied to the FAST-SLOW switch on the front panel to provide the pulse required for time comparisons (see Section 3.5).

"MAKE" and "BREAK" contacts on the 1-second relay and "MAKE" contacts on the 1-minute and 1-hour relays are wired to a socket on the front panel for connection to external circuits, as required.

3.9. Decade Frequency Divider and Readout Meter Units DV2/1 and DV2/2 (Plates 16 & 17)

The Decade Frequency Dividers DV2/1 and DV2/2 are identical units. The 100-p.p.s signal gated through Q6 of the Time Comparator Unit SA4 (see Section 3.5) are applied to the input of DV2/1. Each tenth pulse produces an output pulse from DV2/1, which goes to the input of DV2/2. As the two Decade Frequency Dividers are connected in cascade 100 input pulses are required for one counting cycle, i.e. one complete count occurs each second. If the gate in SA4 is shut off before one whole second has elapsed, the condition of the bistable circuits in each divider unit at that moment is indicated by the reading of its associated meter on the front panel.

Each DV2 unit consists of Q1 and Q2; Q3 and Q4; Q5 and Q6; and Q7 and Q8 connected as bistable multivibrators (see Appendix 2). The zero state of the counter occurs with Q2, Q4, Q6, and Q8 conducting. This is obtained by momentarily breaking the emitter circuits of Q1, Q3, Q5, and Q7 with the RESET microswitch. The first three stages are coupled as binary scalers giving a division ratio of $2^3 = 8$. Diodes CR2 and CR4 and resistor R3, in effect, form a negative AND gate (see Appendix 3), which permits transmission of pulses from the first bistable circuit to the second, providing Q7 is off. On the eighth pulse, Q7 is turned on by a positive pulse from Q6 via C16, and the tenth pulse, which would otherwise trigger the second stage, is now unable to do so. However, in this condition the fourth stage is receptive to a trigger pulse from Q2, via C15, which occurs when Q2 is turned on by the tenth pulse, and is then triggered back to its initial state. The sequence is best illustrated by the table on the decade counter block diagram (see Plate 17) in which 1 denotes the ON state of a transistor and 0 the OFF state. Note that there is one positive pulse out for every ten in, a

positive pulse (or more accurately step) being indicated by a change from 0 to 1 when reading vertically down the output column. From this it is apparent that there are ten different combinations of the bistable ON and OFF states, each of which corresponds to an input pulse between 0 to 9. These are determined by various combinations of ON and OFF outputs of the four bistable circuits.

If weights 1, 2, 4, and 8 are assigned to bistable circuits 1 to 4 respectively, the sum of the weights for bistable circuits in the 0 (OFF) state is equal to the number of pulses counted by the circuit; e.g. after the seventh input pulse, bistable circuits 1, 2, and 3 are 0 (OFF); the sum of the weights assigned to these bistable circuits is 1 + 2 + 4 = 7.

For semi-analogue output to a meter or recorder, it is only necessary to arrange for bistable circuits 1 to 4 to provide currents in the ratio 1:2:4:8 through the meter or recorder when in the 0 (OFF) state, and zero current when in the 1 (ON) state. This is achieved by connecting resistors R36, R37, R38, and R39 with values in the ratio $1:\frac{1}{2}:\frac{1}{4}:1/8$ to the outputs of bistable circuits 1 to 4 respectively. The currents in these resistors are summed in a common line which is connected to the Readout Meter negative terminal; the positive terminal being connected to the emitter -4.5 volt supply.

The count in DV2/2 is stepped on by each tenth pulse, and in DV2/1 by each single pulse. As the pulses occur each 10 milliseconds, the combination of the meter readings indicates the fraction of a second to the nearest 10 milliseconds.

3.10. <u>-6 Volt and -9 Volt Regulated Power Supply Units PP1 and PP2 (Plates 18 & 19)</u>

All units in the NCD2 with the exception of AM2 and AM3 are operated from regulated power provided by either PP1 or PP2. The unregulated 11 to 17 volts supply voltage is applied to the input of PP2, where primary regulation is effected. The -9 volts output from PP2, as well as being distributed to other units as required, provides the input source for PP1, which in turn produces a regulated -6 volt output. The circuits of both PP1 and PP2 are identical except for some component differences to suit the different operating requirements of each regulator.

A constant principle of regulation is employed to control the operation of the series transistor Q2. Q4 is the constant current

generator. Base voltage is held approximately constant by diode CR2. The diode is forward-biased by R8. The current through R6, therefore, is virtually constant. As the collector current $I_c = \alpha I_e$, where I_e is the emitter current, then the collector current also remains constant.

Q3 and Q6 present current-dividing paths for the Q4 collector current. The current-division ratio is determined by the base current of Q6, which is governed by the voltage difference between emitter and base. The emitter is held at a reference voltage by zener diode CR3. The base is connected to voltage divider network R5, R7, and R10. If the regulator output voltage increases, the potential at the base of Q6 increases, thereby increasing the collector current. Since the current through Q4 is constant an increase of current through Q6 causes less current to flow in the Q3 base circuit, and therefore in the Q2 base. As Q2 is in series with the regulated supply load the change in base current reduces the voltage applied to the load, opposing the original increase. Conversely, a decreased voltage across the load increases the voltage applied through Q2 to the load until both are equal. The base current of Q2, then, is independent of variations of its collector voltage, which is the unregulated d.c. supply potential, and it is affected only by changes of voltage across the divider network. As any changes across the divider effect a corresponding current change through Q2 that opposes the initial change, the output of the regulator too is independent of unregulated d.c. input voltage variations, and is held constant at a voltage determined by the setting of potentiometer R7. A large capacitor (C2) prevents the regulating circuit from oscillating due to phase shift. R11 is a dropping resistor for the front panel indicator lamp.

Q1 and Q5 provide an overload cut-out protective facility. Normally Q1 is biased off, the voltage developed across R3 being insufficient to turn it on. If the current through R3 increases, the voltage between Q1 base and emitter increases until finally it is turned on. When Q1 conducts it turns Q5 on. Q5 now shorts the constant current circuit, cutting Q2 and Q3 off, which causes the negative potential on the regulated line to go towards positive COMMON. This forward-biases CR1, which holds Q1 on, even if the current causing the overload now falls below the operating limit of the cut-out circuit. The forward bias on CR1 can be moved by opening the contacts of the RESET switch which

is wired in series with it, allowing the circuit to be restored to normal.

R4, CR1, and R2 form a parallel path with Q2. If the input voltage is too high, CR1 is again forward-biased and Q1 is turned on and the cut-out circuit operates as for an overload current. C1 and R4 provide a time constant which allows the regulator voltage to build up when it is switched on without operating the cut-out. It also prevents cut-out operation by transients. Normally, the output of PP1 is adjusted to 6 volts and PP2 to 9 volts.

3.11. -10 Volt Regulated Power Supply Unit PP3 (Plate 20)

Although the basic principles of the -10 volt regulator circuit (PP3) are the same as in PP1 and PP2, it differs in a number of respects from these units. Because of the load requirements, the series regulator consists of two matched transistors Q6a and Q6b in parallel, and R3 is 4 x 1 ohm, 7-watt resistors in parallel to handle the power dissipation. The cut-out circuits are also different.

Q1 provides protection against current overloading. It is normally switched off, but if excessive current is drawn, the regulator output voltage will drop. If it drops below the 8.2 volts reference voltage at the Q1 emitter maintained by zener diode CR7, Q1 turns on, which switches Q4 on, and shorts the constant current circuit as in PP1 and PP2. Q3 is the constant current generator, with Q5 and Q7 providing the current-dividing paths.

In the case of excessive voltage on the input line, protection is provided by Q2. If the input voltage exceeds 18.2 volts, Q2 is forward-biased and conducts. This turns Q4 on, shorting the constant current generator. Breaking the RESET line restores normal conditions in both current and voltage cut-out operations.

R14 and R15 permit operation of the regulator if the AM3 unit is not plugged in, but adjustments to the regulator should only be made when the AM3 unit is in. R9, C1, and C2 perform the same functions as the equivalent components in PP1 and PP2.

3.12. -90 Volt Regulated Power Supply PP4 (Plate 21)

Several neon indicators are used in the NCD2 and a suitable voltage source for their operation is generated in the PP4 unit. Mounted on the same card is a gating circuit which strikes the radio Time Indicator neon on the TD1 unit.

Q1 and Q2 are connected in a switching circuit which generates a relatively high frequency (approximately 2 Kc/s) square-wave a.c. across the primary winding of transformer T1.

When the -9 volt supply is connected to the circuit, Q2 is forward-biased and current begins to flow in one half of the primary winding. This induces a current in the feedback windings of the transformer, which applies a positive feedback to the base of Q2, which causes a rapid build up of current in Q2 until it saturates. When there is no further change of current, the field about the primary winding collapses, inducing a current in the opposite direction which cuts Q2 off and drives Q1 to saturation, again reversing the process. The result is that the constant switching of current through Q1 and Q2 induces an alternating current in the secondary winding which, when rectified by the bridge rectifier circuit CR1 to CR4 and filtered by R8 and C3, provides a 90-volt source for operating the neon indicators in the Timing Unit. R1 and R2 are base current limiting resistors and capacitors C1 and C2 are incorporated to improve the rise time of the switching waveform.

Voltage-Dependent Resistor R9 suppresses voltage spikes generated by the square wave. Q3 is forward-biased and normally run. It is switched off by the pulse from the 6-millisecond monostable circuit in SA4. While Q3 is on, the potential at the collector is reduced by the current through R6 to a few volts. As the collector is connected to one side of the neon in TD1, the other side of which is at positive COMMON, the voltage applied across the neon is very low and consequently it cannot strike. When Q3 is switched off its collector potential rises to approximately 90 volts and this applied to the neon indicator allows it to strike whenever Q3 is cut off.

Operation of the 6-millisecond monostable circuit in SA4 is triggered by a one-second radio time signal; therefore the neon is struck each second when radio signals are applied, which permits the position of the MILLISECONDS hand on the Time Display Unit TD1 to be observed at the moment of the arrival of a radio time signal.

4. INSTALLATION AND OPERATING INSTRUCTIONS

All circuit adjustments are made before the NCD2 is shipped. Minor adjustments only should be required on installation.

There are no special precautions to be observed in selecting an operating site for the unit except to ensure that the areas around the battery, battery-charger, and the heat-sinks which form the back of the NCD2 chassis, are all freely ventilated.

4.1. Preliminary checks

The following checks must be made before making any connections to the NCD2:

(1) Remove the top cover-plate and make sure all the plug-in cards are firmly located in their correct positions; see the diagram attached to the underside of the top cover, or Plate 22. The cover need not be replaced at this stage.

(2) Check that the 11-16V SUPPLY switch, the Time Display Unit Motor ON-OFF switch, and the 240V 50-c/s ON-OFF switch on the front panel are in the OFF position.

(3) Check that the 7-amp fuse located on right hand side of the front panel is intact.

(4) Check the electrolyte level and specific gravity of each battery cell. Top up with distilled water if necessary. Also check that the battery voltage is within the range of 11 to 16 volts on load.

4.2. Ground connection

No separate ground connection is necessary if the Time Signal Radio Receiver output is to be connected to the NCD2 TIME SIGNAL socket and the receiver chassis is grounded via the mains flex. Otherwise the GROUND connection can be made to the terminal on the front panel.

4.3. Connections to front panel

(1) Check that all plugs which mate with the sockets on the front panel are wired correctly (see Plate 23). Screw the plugs firmly into place.

(2) Connect the RED leads from the 11-16V SUPPLY plug and from the battery charger to the POSITIVE terminal of the battery. Connect the BLACK leads to the NEGATIVE battery terminal. Connect the battery-charger a.c. leads to a 240-volt power-point.

(3) Connect the TIME MARK leads as required, and the POWER OUT lead to the load to be operated from the internally generated 240 volts a.c. The maximum load must not exceed 30 watts.

(4) Connect the TIME SIGNAL lead to a suitable Time Signal Receiver. Care must be taken to see that the shielded braid of this lead is connected to the correct pin on the TIME SIGNAL socket.

4.4. Switching on

(1) Switch the mains supply to the battery charger ON. Depending on the state of the battery select either the HIGH or LOW position of the HIGH-LOW switch on the front panel of the battery-charger. Adjustments to the charge rate will be detailed in an instruction later in this section.

(2) Remove the cover-nut from the 11 to 16-volt SUPPLY ON-OFF switch and switch to ON. Replace the cover-nut. The 6-volt; 9-volt; 90-volt GENERATOR ON; and CRYSTAL OVEN ON indicator lights should all come on. The SYNCH indicator may also be ON. If it is not, remove the cover-nut from either the ADVANCE or RETARD microswitches and momentarily operate the switch. When the switch is released the SYNCH indicator should glow continuously. Replace the cover-nut.

The CRYSTAL OVEN ON light should initially be on. When the oven reaches its operating temperature the thermostat cycles and the indicator light goes out while the thermostat contacts are open. It is therefore normal for this light to come on and go off every few minutes after reaching operating temperature. If the OVEN light is ON but no other light is showing, press the RESET button underneath the 9-volt light, and then the one under the 6-volt light. If an overload has tripped with the initial surge this will restore it.

Note that the 10-volt light DOES NOT come on at this stage.

(3) Switch the motor ON-OFF switch to ON. The sweep-hands of the time display unit will now be set in motion. In the photograph of the front panel (Plate 1), a CLUTCH RELEASE knob is shown. This has been replaced by a motor ON-OFF switch in a modification to the original time display units.

(4) With the load connected to the POWER OUT socket, switch the 240-volt 50-c/s switch ON. The 10-volt indicator should be on and the neon adjacent to the switch should now be struck. If neither of these indicators is working press the RESET button under the 10-volt indicator.

4.5. Checking the voltage regulator adjustments

Connect a voltmeter set to read 10 volts F.S.D. between POSITIVE COMMON (NCD2 chassis) and a convenient -6volt point. The top of either choke on the oscillator unit is readily accessible (see Plate 24). If necessary adjust to exactly 6 volts by turning the adjustment screw on R7 on the PP1 unit.

Now check that the -9 volt supply is approximately correct. The meter can be connected between the chassis and the top of R2 on the SA4 unit (see Plate 25). Do NOT adjust the PP2 voltage. Final adjustment is made to this regulator when the readout meters are checked.

With the meter between chassis and the -10 volt monitoring point on the PP3 unit (see Plate 26) check that the voltage is between 9.8 and 10 volts. Adjust, if necessary, with R7 on the PP3 unit.

4.6. Checking time-mark operations

No adjustment should be necessary to the time-mark relay circuits. The following instructions are intended as a guide should the relays not operate in their correct sequence.

If the time-mark relays are connected to a system which can be readily observed, the operation of the relays can be checked using this system. Alternatively a meter, set to read resistance, can be connected to the appropriate pair of MAKE contact leads from the TIME MARKS socket (see Plate 23 for pin numbers of each relay). Proceed as follows:

(1) Switch the time display unit motor OFF.

(2) Manually rock the sweep-hand on the MILLISECOND dial about 30° on either side of the 0 graduation. The 1-second relay should operate each time the hand crosses the 0 mark. If it does not operate, rotate the sweep-hand through a full revolution. If the relationship between the sweep-hand and the slotted disc on the same shaft has been altered the relay will operate each time the light gate is triggered. In this case locate the position where the relay operates as the hand is moving in a clockwise direction. Loosen the screws of the locking bar on the boss of the sweephand. Taking care not to alter the position of the shaft, set the pointer on the sweep hand to 0 and tighten the locking bar securely. Repeat the process until the 1-second relay operates as the pointer reaches 0.

If the relay fails to operate at all, the most likely cause is failure of the lamp which provides the light source. This can be checked without removing the TDI unit. The design of the lamp holder allows light to be seen from the rear of the holder. Each of the four light sources can be checked and the lamps replaced if necessary.

(3) When the 1-second relay is operating correctly, check the SECOND sweep-hand.

It is important to note that incorporated in the mechanism of this sweep-hand is a 'one-way' clutch which permits the hand to be freely moved in the clockwise direction only. NO ATTEMPT SHOULD BE MADE TO MOVE IT COUNTERCLOCKWISE. The relative position of the hand to the slotted disc will almost certainly be altered if this is done. Attach the special winder (located in the left hand lower corner of the Time Display Unit) to the SECOND hand for setting the Time Display.

With the MINUTE hand at any position except 0, set the SECOND hand to 0. Now manually set the MILLISECOND hand to 0. The 1-minute relay should now operate continuously, holding in for two seconds each time it is triggered. If it does not do this check that the light

from the lamp is passing through the slot in the disc on the SECOND shaft on to its photo-transistor. Adjust the position of the sweep-hand, if necessary, so that it is at 0 when the light beam triggers the photo-transistor. Note that both the MILLISECOND and SECOND sweep-hands must be at the 0 position for the 1-minute relay to operate.

(4) Set the Time Display so that the MILLISECOND, SECOND, and MINUTE hands are all on 0 and so that the HOUR hand is at any position other than the time when a six-hourly omission is programmed. The 1-hour relay should now operate continuously, holding in for four seconds each time it is triggered. If not, check as previously for the SECOND hand adjustment.

(5) Set the Time Display about 15 seconds before a six-hourly omission (usually 000; 0600; 1200; and 1800 hours G.M.T.) and switch the motor ON. There should be no 1-minute or 1-hour relay operation as the hand passes 0. If there is, check the position of the slotted disc on the HOUR shaft. Adjust if necessary. The other three six-hourly omissions can be checked on a recording made over 24 hours.

4.7. Checking readout meters

With the Time Display motor ON set the FAST-SLOW switch located below the 10-millisecond meter to FAST. Press the RESET switch adjacent to, and to the left of the FAST-SLOW switch, then release. The first 1-second relay pulse after resetting will commence the counting process. Then change the switch to SLOW. The next 1-second relay pulse will stop the count at some random fraction of a second which will be displayed on the readout meters. The meters read incremental steps from 0 to 9. Each step on the left-hand meter is equivalent to 100 milliseconds, and the right hand meter 10 milliseconds. Repeat this operation until a wide range of meter readings has been observed. If both meters are reading high or low adjust the 9 volt regulator with R7 on the PP2 unit until the counts of 9 on each meter are indicated correctly.

The top vover-plate can now be screwed down. If it is convenient allow several hours for the NCD2 to warm up to its operating temperature.

4.8. Function of the FAST-SLOW switch

It is important that the operation of the FAST-SLOW switch be clearly understood to enable accurate time corrections to be made.

In the FAST position the count on the Readout Meter is commenced by a 1-second relay pulse and stopped by a 1-second radio pulse, i.e. the fraction of a whole second that the clock is ahead of the radio time signal is displayed on the readout meters.

In the SLOW position a 1-second radio signal starts the count and it is stopped by a 1-second relay pulse, i.e. the display indicates the number of milliseconds later that the clock pulses occur in relation to the radio signals.

This can be demonstrated, when a good radio signal is available, by observing a readout in the FAST position and then one in the SLOW position. The two readings added together make a total of 1 second (or more usually, since the count on both is to the nearest 10 milliseconds, the total is 1.010 seconds).

4.9. Setting the Time Display to correct time

(1) Switch the Time Display motor OFF. Attach the special winder to the SECOND hand and wind on in a CLOCKWISE DIRECTION ONLY until the indicated time is five or ten minutes ahead of actual time. Set the MILLISECOND hand at about 200 milliseconds. Note: The HOUR hand can be loosened on its shaft and altered in steps of EXACTLY six hours, so it should never be necessary to wind the Time Display on more than six hours.

(2) With the output of a time-signal radio receiver connected to the TIME SIGNAL socket, tune the radio to a time signal transmission. The PMG station VNG at present only identifies the first minute of each hour, so unless the clock is to be set on the hour it is better to use WWVH or JJY transmissions on 10 or 15 Mc/s. Signals from VNG on 12.005 Mc/s can be used to correct the MILLISECONDS error.

(3) When the radio signal indicates the same time as the Time Display, switch the motor ON. The NCD2 time should now be within half a second or so of correct time.

(4) Observe carefully the position of the SECOND sweep-hand when a one-minute radio signal is heard. From this observation it can be determined whether the indicated time is slightly fast or slow.

If it is fast remove the cover-nut from the RETARD microswitch. Increase the radio receiver output level until the neon mounted behind

the MILLISECOND dial strikes regularly with each 1-second radio signal. Under poor conditions the neon will not strike when the signal fades, or may strike irregularly with random noise. The output level of the receiver has to be adjusted for optimum operation under these conditions. Switch the FAST-SLOW switch to FAST and take several consecutive readout readings. If the majority of them are the same, i.e. the count is being stopped by a 1-second radio signal and not by random noise pulses, press the RETARD switch for a few moments, release, and take another set of meter readings. Repeat until the readout is zero on both meters. Switch to SLOW and check the readout in this position. It should be 000 or 010 milliseconds.

CAUTION: If the signal level from the receiver is set too high a constantly repeated reading of 10 or 20 milliseconds will be displayed because the counting is being started or stopped by noise pulses. A visual check of the readout can be made by observing the position of the MILLISECOND sweep-hand when the neon indicator is struck with 1-second radio signals. With a little practice this can be judged quite accurately.

Replace the cover-nut when the clock is finally corrected. If the clock is slow the procedure is the same except that the ADVANCE micro-switch is operated.

4.10. Adjusting the clock rate

Allow the NCD2 to operate for several days. Make daily observations of the error compared with radio time. As the temperature inside the NCD2 stabilises, the rate of the clock will show a tendency towards a steady daily rate of change.

If the daily rate requires adjustment, remove the screws from the top cover-plate and push the cover-plate back just far enough to expose the oscillator (01) unit. This is to prevent as far as possible a large temperature change inside the unit. The special tool (located in a spring clip on the chassis wall next to the TD1 unit) is inserted in the variable capacitor C2 of the 01 unit. If the rate is to be decreased, turn the adjusting screw CLOCKWISE or for a faster rate turn it COUNTER-CLOCKWISE. One full turn is approximately equal to a change in rate of 250 milliseconds per day. The actual amount depends on the relative position of the plates of the capacitor.

Replace the special tool in its holder and replace the top cover-plate. Periodically adjust the rate of the clock until the most satisfactory performance is obtained.

4.11. Adjusting the charge rate of the battery-charger

(1) With the HIGH-LOW switch on the battery-charger on HIGH adjust the transformer secondary tapping in conjunction with RV1 (Plate 27) for a charge rate of 15 to 18 amps.

(2) Measure the current drawn by the NCD2 with its normal full load. Switch the HIGH-LOW switch to LOW. If a 24-hour mains supply is available adjust the rate of charge to about $\frac{1}{2}$ amp more than the normal drain with RV2.

CAUTION: Do not make any adjustments to the battery-charger without first disconnecting it from the mains supply. If the mains supply is less than 24 hours per day the charge rate can be calculated as follows:

EXAMPLE: If the NCD2 current drain is 5.7 amps and the mains supply is available for 14 hours per day;

Then the total drain in one week = 5.7 x 168 amp-hours
= 957.6 amp-hours

Charging time available in 1 week= 14 x 7 = 98 hours

Then the rate of charge required = $\frac{957.6}{98}$ amps
= 9.77 amps

Plus 10% compensation for losses = 9.77 + .98
= 10.75 amps

Therefore a charge rate of $10\frac{3}{4}$ amps should keep the battery charged.

4.12. Brake tension

A brake is fitted to apply pressure to the Time Display unit MILLISECOND shaft. This prevents flywheel action in the gear-train causing over-running of the coupling mechanism between the gear train and the motor.

If the MILLISECOND sweep-hand does not run smoothly through each revolution, remove the TDU unit and adjust the brake tension until this condition is obtained.

4.13. Routine checks during operation

A daily comparison with radio time signals is advised. Corrections can be made when required as outlined in Section 4.1, paragraph 4.

If it is found that the clock rate requires occasional adjustment as the crystal ages refer to Section 4.10.

A weekly check of the electrolyte level in each of the battery cells is recommended. Cells should be topped with distilled water if the level falls below the maker's recommended minimum.

5. MAINTENANCE

5.1. General

Prolonged tests with the NCD2 operating under remote field conditions has established that reliable operation of the clocks can be obtained with a minimum of maintenance.

The only moving parts (except for the relay armatures on the SA3 unit) are contained in the Time Display Unit (TD1) mechanism. Regular inspection of the gear-train and synchronous motor bearings should be carried out and replacements made at the first sign of wear.

If the load on the 240-volt 50-c/s power output is less than 15 watts, the voltage-dependent resistor across the secondary winding of the AM3 power output transformer can be removed without affecting the performance of the unit.

Wherever possible, waveforms and voltages are shown on the circuit to assist servicing and location of faults.

A complete set of spare plug-in cards is supplied to enable continuity of operation to be maintained as far as possible.

5.2. Fault-finding

It is beyond the scope of this section to attempt to list every fault which may occur in the NCD2 at some time or another. The operation of the Time Display Unit sweep-hands, the indicator lamps on the front panel, and time marks, provide excellent monitoring facilities. Observation of these can assist in determining whether or not there is any malfunctioning of the equipment and, if so, indicate the circuit in which the fault is most probably located.

For example, if the 10-volt light is on and the sweep-hands are operating normally but there is no 240-volt 50-c/s light, the fault would most likely be in the AM2 or AM3 units. On the other hand if the 10-volt and the 240-volt 50-c/s lights are out and the Time Display is operating normally, the fault would most probably be in the -10 volt Regulator Unit (PP3), or due to low battery voltage.

Again if the SYNCH light is out but the 90-volt GENERATOR light is on, the Divider Units (DV1/1 and DV1/2) are probably out of synchronisation, whereas if both are out it could mean that the 90-volt Generator Unit (PP4) is unserviceable.

It must be borne in mind that each relay operation is dependent on gating signals coinciding. The absence of time marks altogether can result from failure of several circuits, but if minute time marks appear and there are no hour marks the first circuit to check is the lamp providing the light gate for the 1-hour pulse, and so on.

A brief study of the functions of each indicator light, time-mark operation, and plug-in circuit is invaluable in diagnosis of faults. It is recommended that the operator of the NCD2 become familiar with these functions.

APPENDIX 1

THE COOKE-YARBOROUGH MONOSTABLE MULTIVIBRATOR

General description

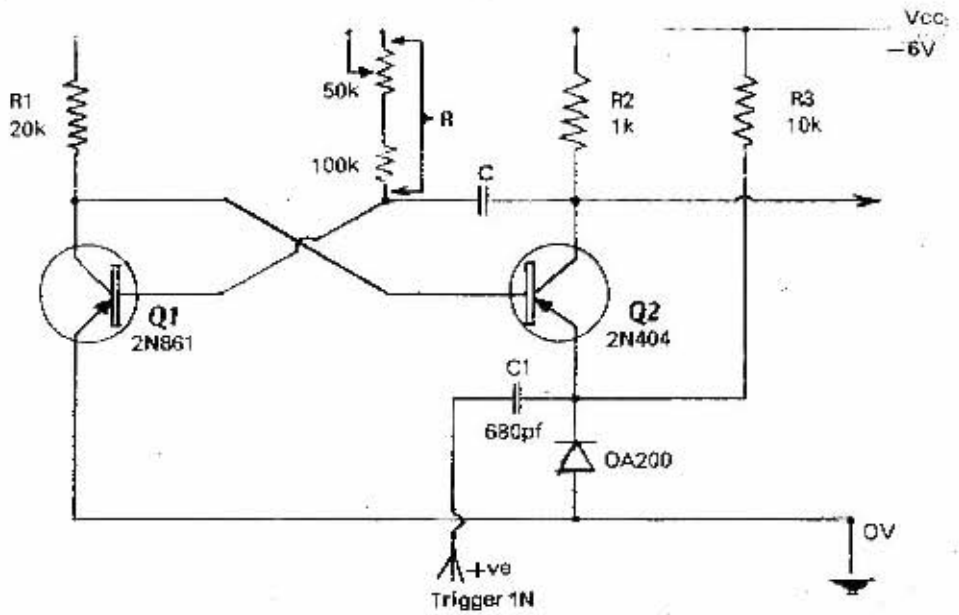


Figure 2

In the stable state Q1 is on (saturated) and Q2 off. A positive trigger pulse causes Q2 to turn on and Q1 to turn off for a time determined by time constant RC. At the conclusion of this quasi-stable period the system relaxes back to its stable state.

The stable state

Q1 draws base current through R, ($I_{b1} \approx V_{cc}/R$), saturating if $\beta 1 \geq R/R_1$. Q1 collector is thus maintained at approximately -0.2 volt, reverse biasing the base-emitter junction of Q2. The Q2 emitter is held at approximately -0.5 volt because of the forward biased OA200 silicon diode.

The resistance seen by the base of Q2, i.e. the saturation resistance of Q1, would be typically a few hundred ohms. Even if this resistance were 1000 ohms, Q2 base current caused by emitter and collector leakage currents would have to be at least (0.5 - 0.2)/1000 = 330 microamps, before leakage could turn Q2 on. This value is much larger than is normally found in low current germanium switching transistors at 60°C.

The quasi-stable state

If Q2 starts to turn on, regenerative switching will occur providing the circuit, considered as a positive feedback amplifier, has a loop gain greater than unity. If switching is sufficiently fast the leading edge of the positive step at Q2 collector is transmitted across C to the base of Q1. The voltage across a capacitor cannot change instantaneously. Q1 base-emitter junction is thus reverse biased by about $(V_{cc} - \frac{1}{2})$ volts. This base potential reaches approximately zero volts, Q1 starts to turn on, regeneration occurs and the system returns to its stable state. While Q1 is off, Q2 is saturated by base current drawn through R1.

Effect of leakage in Q1

If leakage occurs through the collector-base junction while Q1 is off, the effective decay time constant becomes R'C, where $R' = Re_b/(Ri_{bL}+e_b)$, where e_b and i_{bL} are the instantaneous values of base voltage and leakage current. As leakage current is a function of temperature, the decay time constant will be temperature dependent unless leakage is eliminated or made very small. Low leakage is obtained by using a silicon transistor for Q1.

For quasi-stable period greater than about one second it is convenient to make C an electrolytic capacitor, which provides an additional leakage path. Solid tantalum electrolytics leak less and are more stable against temperature and ageing than aluminium foil types and should be used when moderate precision is required.

The positive side of the electrolytic connects to the base of Q1. (Reverse for NPN circuit).

Choice of transistors

Ideally, both Q1 and Q2 should be high-gain, high-frequency transistors to ensure fast switching, with consequent minimum attenuation of the pulse transmitted across C.

Leakage requirements have already been dealt with.

The positive pulse turning Q1 off should not break down the base emitter junction, hence a transistor is required having $V_{be\ max}$ at least equal in magnitude to the supply voltage.

Triggering

The trigger signal should be a positive step or pulse having fast rise time, for minimum attenuation across coupling capacitor C1, and

amplitude large enough to overcome the reverse bias on Q2. Trigger signals less than $\frac{1}{2}$ volt will be shorted to ground via the forward biased OA200. Trigger signals greater than $\frac{1}{2}$ volt will reverse bias the OA200 and forward bias Q2 emitter-base junction. The positive trigger pulse at Q2 emitter will decay with time constant set by C1 and Q2 emitter resistance. Thus both initial trigger amplitude and the value of C1 must be high enough to ensure that Q2 is forward biased throughout the switching time, i.e. for a few microseconds.

For the circuit shown, minimum trigger amplitude should be about 3 volts with minimum rise time of a few microseconds.

Waveforms

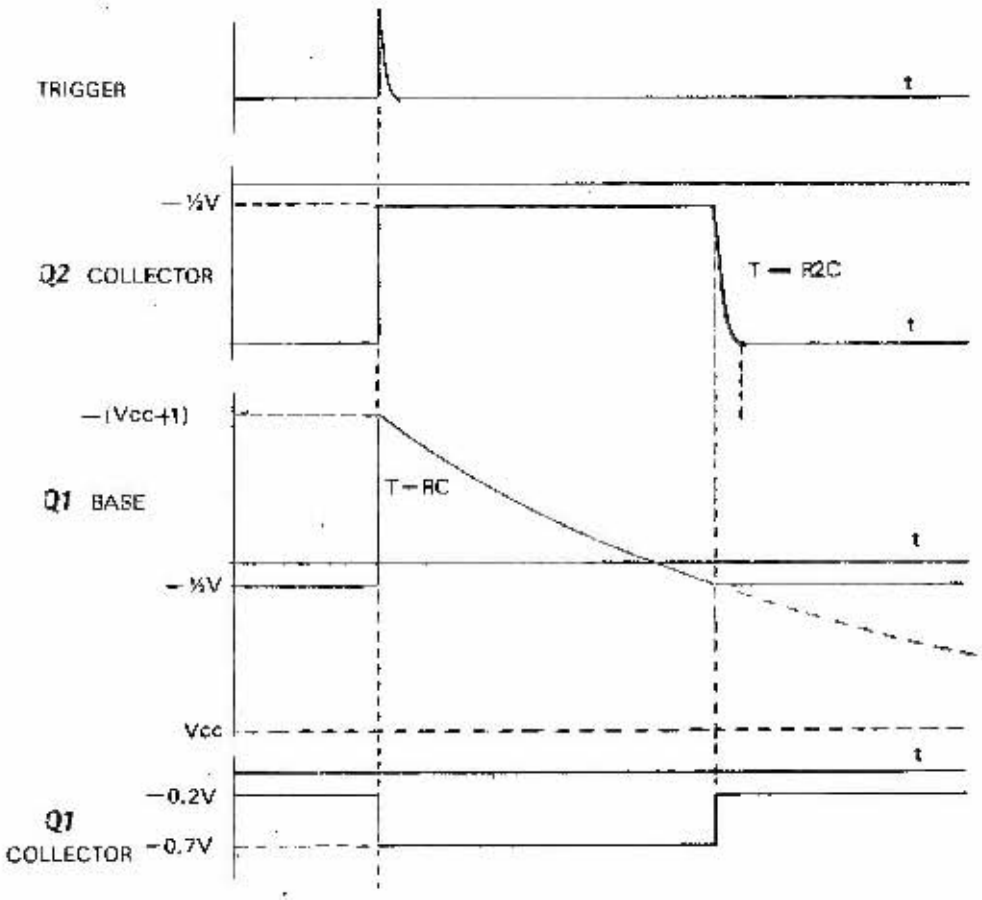


Figure 3

Notes:

When Q2 turns off, the collector does not fall to V_{cc} volts instantaneously, but does so with time constant R2C.

Q1 collector voltage is clamped at about -0.7 volts when Q1 is off because of the direct connection to the forward biased Q2 base.

The quasi-stable period

Neglecting leakage, base-emitter voltage drops, attenuation through C, and the drop across the OA200, the quasi-stable period would be

$$T = RC \log_e 2 = 0.693RC$$

(T in milliseconds, R in Kilohms, C in microfarads.) This period is slightly reduced by combinations of the above factors, but is usually used as a basis for design. Accurate period adjustment is provided by the variable portion of R.

Factors determining precision

For high timing precision and repeatability:

(1) R and C should be stable and possess either zero or equal and opposite temperature coefficients.

(2) All leakage currents should be constant.

(3) Switching times should be constant.

(4) Q2 collector loading should be constant.

(5) Trigger amplitude and rise time should be constant.

(6) V_{cc} should be constant and as large as possible to give steepest possible slope to the timing wave-form.

The monostable circuit as a frequency divider

If trigger pulses be applied at pulse repetition period t to a monostable circuit having quasi-stable period T, frequency division will occur if $T > t$.

In general, for a dividing ratio n,

$$T = t(n - 1 + x),$$

where n is integral and $0 < x < 1$.

This comes about because trigger pulses can have no effect when the system is in its quasi-stable state. After returning to the stable state, however, the next trigger pulse will again produce the quasi-stable state. Waveforms for divide by 10 from 100 kc/s are shown in Figure 4.

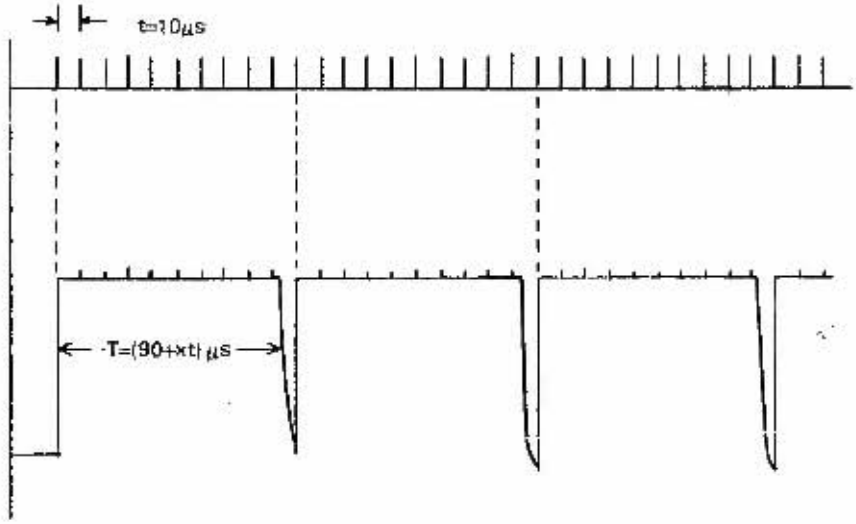


Figure 4

Trigger pulses reflected on the collector waveform are useful for setting up. The value of T is adjusted until there is one monostable cycle for every 10 trigger pulses. The exact value of T for maximum reliability is not 95μs as may be expected, but somewhat less than this; about 93μs. This is a consequence of the finite fall time of the collector waveform. However, T can still vary by about ±5μs from its optimum value without changing the division ratio, i.e., a time constant drift of ±5% can be tolerated.

In practice it is best to set T half way between the values obtained when the system just ceases to divide by 9 and just commences to divide by 11. If T is near the upper extreme of its allowable excursion, i.e., almost dividing by 11, a transition mode may occur with alternate periods differing slightly but still dividing by 10. Again, this is caused by the finite fall time at Q2 collector.

This fall time is the main limitation for high frequency operation. Even at 100 kc/s input, the output should be coupled to the next divider via an emitter follower to prevent increase in fall time by capacitive loading.

Advantages of monostable dividers

(1) As the system is in the quasi-stable state for most of the time, susceptibility to stray noise pulses is low.

(2) For a given division ratio, the number of components required is less than for most other dividers.

(3) If the input fails there is no output, i.e., the circuit cannot free run.

Limitations of Circuit

(1) Unlike biscale dividers, the monostable circuit cannot be used as a counter.

(2) The division ratio is frequency dependent.

(3) Maximum division ratio for reliable operation is 10.

(4) Upper limit on trigger frequency is just above 100 kc/s.

(5) For output frequencies less than about 2 c/s, the performance depends on the stability of an electrolytic capacitor.

APPENDIX 2

THE BISTABLE MULTIVIBRATOR

General Description

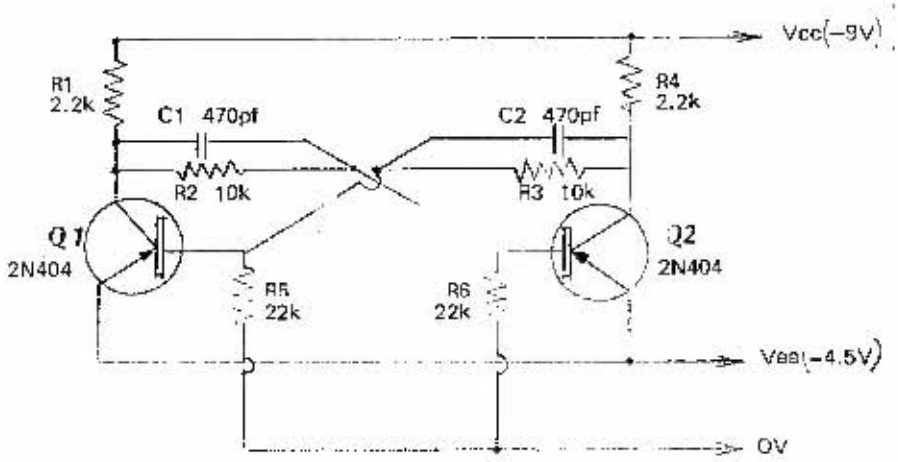


Figure 5

The circuit has two stable states: Q1 on (saturated) and Q2 off; and vice versa.

Assume Q1 is on. The potential at Q1 collector is approximately V_{ee} and the voltage developed across R6 is R6 $V_{ee}/(R2+R6)$. This is more positive than V_{ee}, hence Q2 base-emitter junction is reverse biased and Q2 held off. Q1 base current is $(V_{cc} - V_{ee})/(R3 + R4)$, which for saturation must be equal to or greater than the collector current divided by the transistor current gain.

$$\text{i.e.} \quad (V_{cc} - V_{ee})/(R3 + R4) \geqslant (V_{cc} - V_{ee})/\beta 1 \quad R1$$

$$R3 + R4 \leqslant \beta 1 \quad R1$$

Similarly, for the other stable state,

$$R1 + R2 \leqslant \beta 2 \quad R4$$

R5 and R6 are determined by the maximum value of collector leakage current, I_{co}. When Q1 is off, R5 must be such that R5 I_{co} (i.e. voltage developed across R5 by leakage current) is more positive than V_{ee}, thus preventing leakage from turning Q1 on. R5 and R6 cannot be made too low, however, as the large resulting turn-off bias on the off transistor would render the circuit difficult to trigger from one state to the other.

Switching

Assume Q1 is on and Q2 off. If, for some reason the base of Q1 starts to go positive, Q1 will start to turn off and its collector potential will change in a negative direction. This change is transmitted to the base of Q2 via R2 and, if Q2 base potential goes sufficiently negative to overcome its reverse bias, Q2 will start to turn on. Thus a positive going potential is produced at Q2 collector and is transmitted to Q1 base via R3, augmenting the initial change. The circuit behaves like a positive feedback amplifier, and if the loop gain is greater than unity the process will continue of its own accord until Q1 is off and Q2 on, i.e. the circuit is regenerative.

To increase switching speed, speed-up capacitors C1 and C2 are often used. These ensure that the leading edge of the switching pulse is transmitted from collector to base with negligible attenuation. Typical turn-on time for the circuit shown is 0.5 microseconds.

Triggering

In B.M.R. circuits, triggering is usually accomplished by injecting a positive pulse into the base of the on transistor. To achieve this the following circuit is added to each transistor of the basic circuit.

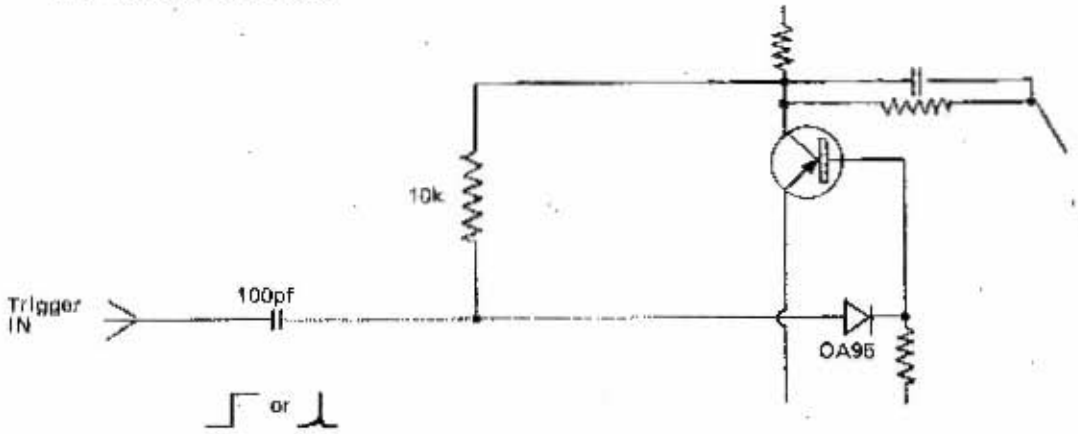


Figure 6

This circuit allows positive pulses or the leading edge of a square wave to trigger the bistable circuit. When Q1 is on, the OA95 trigger diode is slightly forward biased. (Q1 collector is approximately 0.1 volt more positive than base). A positive trigger pulse will reverse bias the diode and thus be blocked.

When Q1 is off, the trigger diode is reverse biased by an amount equal to the difference between collector and base potentials. A positive pulse, even if it overcomes this reverse bias, will only tend to turn Q1 off further. A negative pulse will increase the trigger diode reverse bias and is thus prevented from reaching the base of Q1.

The two trigger inputs may be independent, each being derived from a separate source, or they may be connected together and fed from a common source in which case the circuit will act as a binary scaler, i.e. will divide by two, as shown in Figure 7.

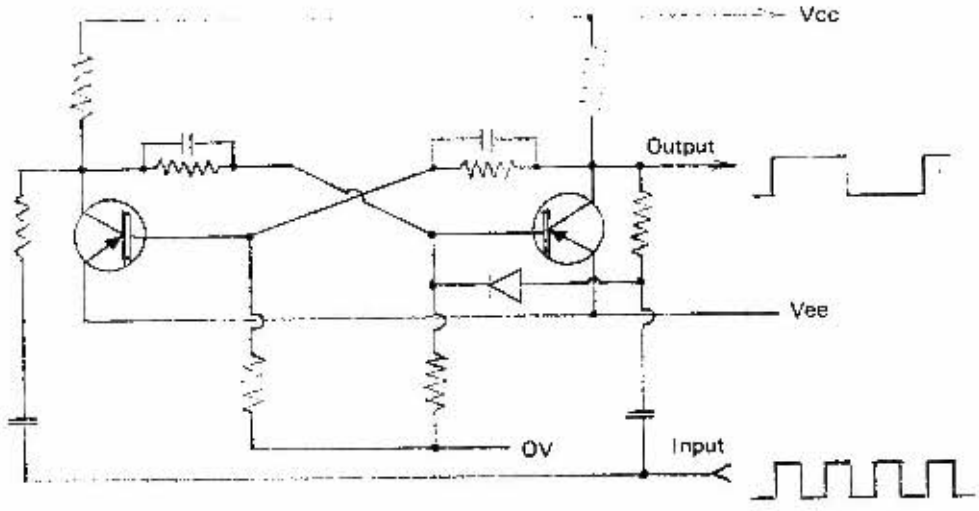


Figure 7

Under these conditions each successive trigger pulse is automatically steered to the base of the on transistor.

Assume Q2 is on. The next trigger will turn it off and the following turn it on again, i.e. there is one positive-going output step for every two input pulses. If n such stages are cascaded, division by 2^n results.

APPENDIX 3

GATING CIRCUITS USED IN THE NCD2

Photonic and time pulse gates (Plates 13, 14, & 15)

Note that the photo-transistors give positve output pulses when illuminated, but these are subjected to a NOT operation before being applied to the various gates. This is simply achieved by using the phase inversion inherent in a common emitter amplifier (Q2, Q6, Q7, Q9, Q11 in SA2).

Gate A Negative NAND. The two inputs are the bases of Q3 and Q4 in SA2. Output is from Q3 collector, where the potential remains at -6volts until both Q3 and Q4 are turned on by negative signals at their bases. This can only happen when both the hour and six-hour light gates operate. At this time, Q3 collector rises to about $-\frac{1}{2}$ volt, providing a positive-going signal for input to gate C.

Gate B Negative AND. The two inputs are from the collector of Q7 (SA2) and emitter of Q6 (SA3). Output is from Q7 (SA2) collector. When the one-hour light gate is unenergised, Q7 is on, i.e. one input is positive. This means that the output is also positive, thus preventing positive pulses at the second input from passing through tho gate. This happens because CR7 (SA3) becomes reverse biased by the positive potential on Q7 collector.

When the one-hour light gate is energised, Q7 turns off, providing one 'true' input to the gate. The output will then follow the second input, as CR7 can now become forward biased by a positive signal on its anode.

Thus the one-hour monostable circuit can only be triggered when both the one-hour light gate and the one-minute monostable circuit are energised.

It should be noted that the positive-going output of gate B, which occurs when illumination is removed from the one-hour photo-transistor, has a rise-time which is far too long to trigger the one-hour monostable circuit.

Gate C Negative AND. The operation of this gate is the same as that of gate B, except that a third input is applied from the output of gate A. As previously shown, gate A output is positive when the six-

hour light gate operates. This causes gate C to be inhibited, thus preventing the one-minute and one-hour monostable circuits from operating. Inhibiting occurs because of the forward bias on CR3 (SA2), which prevents gate C output from going negative.

Gate D Negative AND. Inputs are at the base and emitter of Q12 (SA2). Output is from Q12 emitter.

When the one-second light gate is unenergised, Q11 collector is at the positive level, causing Q12 to be reverse biased. Thus 50-c/s input signals on Q12 base cannot reach the output of the gate.

However, Q12 becomes forward biased when the one-second light gate is energised and gate D output can follow the signal on Q12 base. The first positive pulse from this signal triggers the one-second monostable. Because the light gate pulse and the monostable pulse are of the same duration, the monostable circuit can only be triggered once each time the light gate is energised.

Divider synchronising gates (Plate 4)

Negative AND Gate. Inputs are Q5 base and CR6 anode. Output is CRC cathode.

When the 12-millisecond monostable circuit is off, Q5 base is negative. As Q5 is an emitter follower the emitter is also negative. CR6 is then forward biased and signals from the 100-kc/s oscillator can pass through to the dividers.

When the 12-millisecond monostable circuit operates, Q5 emitter becomes positive, CR6 is reverse biased, and signals can no longer reach the dividers.

Negative NAND Gate. Inputs are R19 and R20. Output is Q6 collector.

The operation of this gate is the same as that of gate A in the previous section.

Time comparator gate (Plates 7 & 8)

Negative AND Gate. Inputs on the bases of Q5 and Q6 emitter followers. Output is from the common emitter resistor R19.

When bistable circuit 2 is off, Q5 base is negative and Q5 almost fully turned off. The signal on Q6 is then able to appear at the gate output.

When bistable circuit 2 is on, however, Q5 is saturated and the common emitter point is clamped to the positive supply line, thus preventing any signal on Q6 base from reaching the counter input.

PLATES TO ACCOPMANY

RECORD No. 1968 / 32

Crystal Timing Unit Type NCD 2

To Accompany Report Number 82/132

CRYSTAL TIMING UNIT NCD2

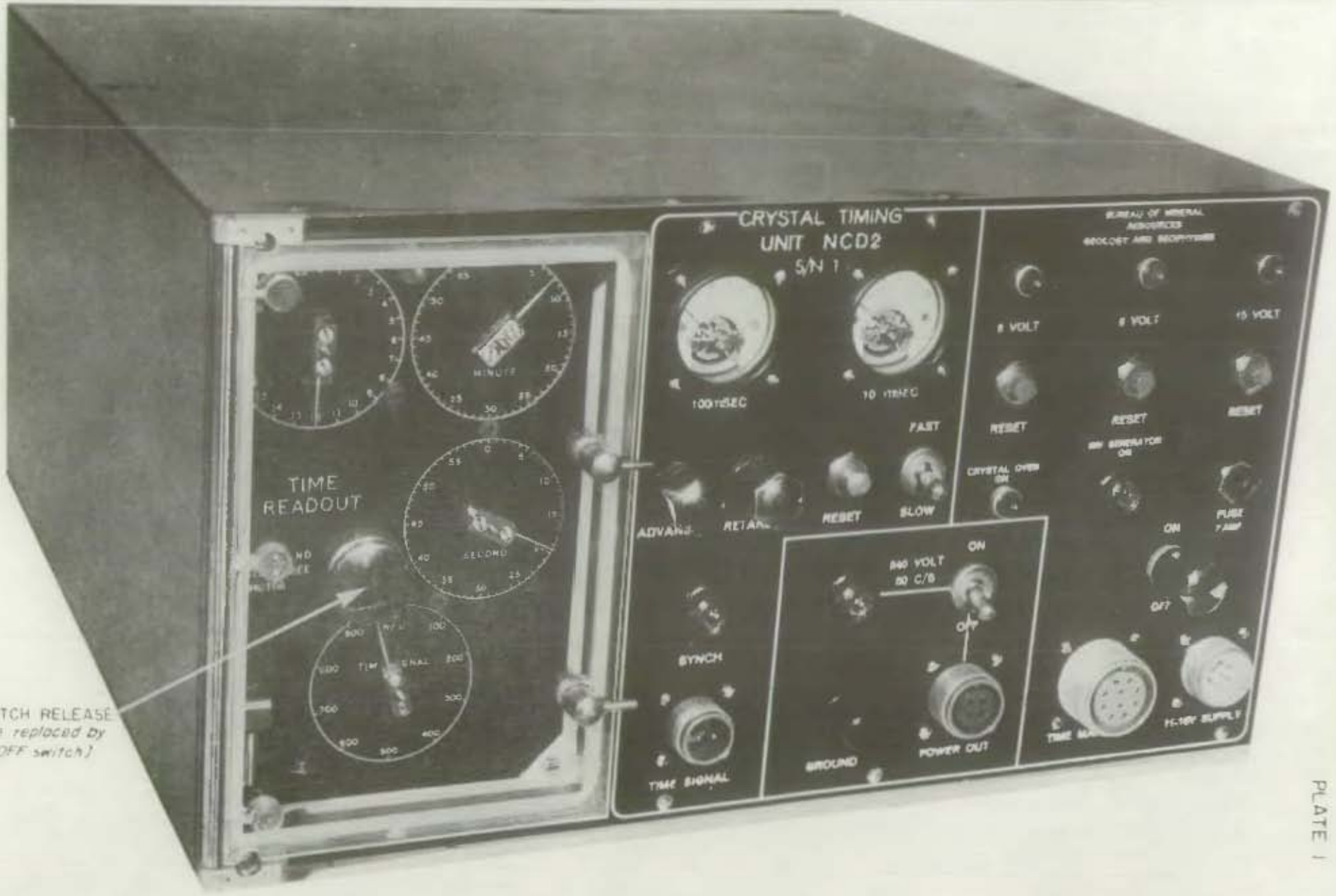
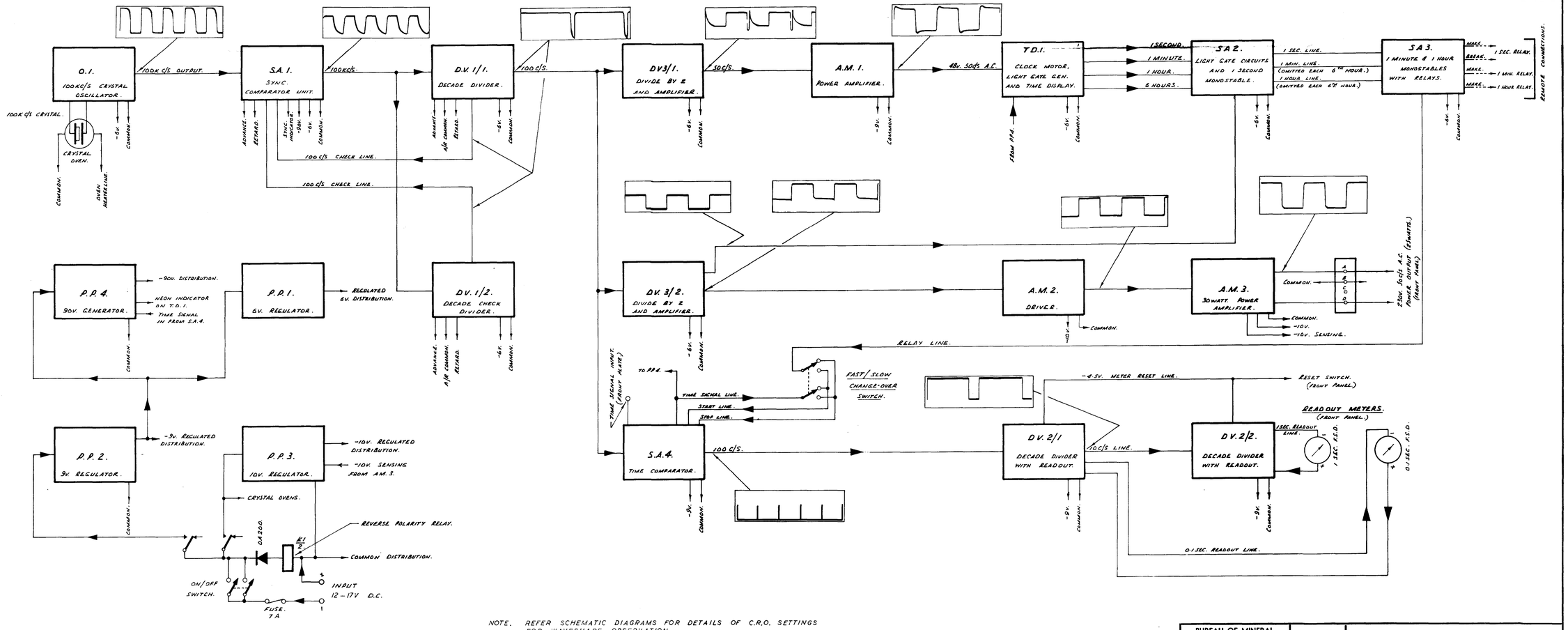


PLATE I

G82/3-101

	DATE	NAME
Orig.	4-5-64	R. G.A.N.
Amend.	7-7-64	N D J

PLATE 2



NOTE. REFER SCHEMATIC DIAGRAMS FOR DETAILS OF C.R.O. SETTINGS FOR WAVESHAPE OBSERVATION.

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G82/3-102	BLOCK DIAGRAM OF NCD 2

TO ACCOMPANY RECORD No 1968/32

COMPONENT LIST.

CONNECTOR.

P1	SOURIAU 8140-02 MALE 5 PIN VOCAB. BKZ198	

TRANSISTORS.

Q1 Q2 Q3 Q4	TRANSISTOR TYPE 2N404 VOCAB. BVT/2N404	

DIODES.

CR1 CR2 CR3 CR4 CR5	SILICON DIODE TYPE OA200 VOCAB. BVD/OA200	

CHOKES.

L1	15 mH "Q" PLUS TYPE LR31P	
L2	2.5 mH "Q" PLUS TYPE RFC2	

Both chokes available ex R.W STRANE PTY.LTD. Melbourne.

CAPACITORS.

C1	DUCON "SIMPLEX" SILVERED MICA TYPE MS NOM. 68PF VOCAB. BCM5680	
C2	PISTON TRIMMER CAPACITOR. JFD ELECTRONICS CORP. USA MAX.C SEALCAP SERIES TYPE MC606 1-60PF	
C3	PHILIPS POLYESTER TYPE C296 0.01 MFD VOCAB. BC01103	125V.
C4	DUCON STYROSEAL TYPE DFB600 100 PF VOCAB. BCP6101	600VW
C5 C10 C11	PHILIPS POLYESTER TYPE C296 22000 PF VOCAB. BC01223	125VW
C6	DUCON STYROSEAL TYPE DFB616 2200 PF VOCAB. BCP6222	600VW
C7 C8	PHILIPS POLYESTER TYPE C296 33000 PF VOCAB. BC01333	125VW
C9	DUCON STYROSEAL TYPE DFB608 470 PF VOCAB. BCP6471	600VW

RESISTORS.

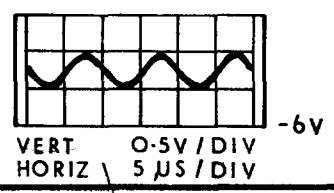
Following resistors to be WELWYN "METOX" ½ WATT TYPE F20

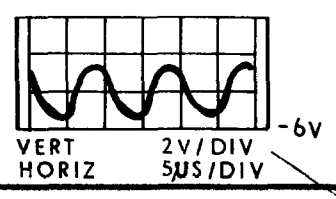
R1	200K OHMS
R2	62K OHMS
R3	39K OHMS
R4	3K OHMS
R5	3.9K OHMS
R6	6.8K OHMS
R7	1K OHMS
R8	10K OHMS
R9	2.7K OHMS
R10	18K OHMS
R11	180 OHMS
R12	7.5K OHMS
R13	820 OHMS
R14	4.7K OHMS

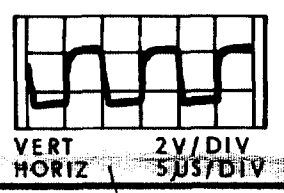
CRYSTAL X1. QUARTZ CRYSTAL UNIT. PYE TYPE Q14-X 100KC/S ± 3 C.P.S
EXTERNAL SERIES CAPACITOR 100 PF.

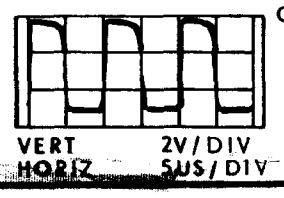
OVEN. CRYSTAL OVEN 75 degrees C. 13 VOLT. JAMES KNIGHTS TYPE JK09S130 PART No. 908-4541. Available ex PYE.

	DATE	NAME
Orig.	13 · 8 · 63	N D J
Amend.	24 · 12 · 63	N D J
	19 · 6 · 64	N D J









BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS

Drawing No. G82/3-103

CRYSTAL OSCILLATOR UNIT 01

PLATE 3

TO ACCOMPANY RECORD No 1968/32

COMPONENT LIST.

CONNECTORS.

P1 P2 SOURIAU 8140-02 MALE 5 PIN VOCAB. BKZ198

TRANSISTORS.

Q1 TRANSISTOR TYPE 2N861 VOCAB. BVT/2N861

Q2 Q3 Q6 Q7 TRANSISTOR TYPE 2N404 VOCAB. BVT/2N404

Q4 Q5 TRANSISTOR TYPE 2N388 or 2N535 VOCAB. BVT/2N388

Q8 TRANSISTOR TYPE 2N398A VOCAB. BVT/2N398A

DIODES.

CR1 CR2 CR3 SILICON DIODE TYPE OA200
CR4 CR5 CR7 VOCAB. BVD/OA200

CR8 GERMANIUM DIODE TYPE OA95
CR6 VOCAB. BVD/OA95

CR9 SILICON ZENER DIODE TYPE 24.7T5
VOCAB. BVD/24.7T5

CAPACITORS.

C1 C5 PHILIPS POLYESTER TYPE C296 125V.
0.1MFD VOCAB. BC01104

C2 C3 DUCON STYROSEAL TYPE DF5610 600V.
680 PF VOCAB. BGP6681

C4 TANTALUM ELECTROLYTIC SPRAGUE TYPE
150D 107x0015 100MFD 15V.

RESISTORS.

Following resistors to be WELWYN "METOX" ½ WATT TYPE M20

R1 R19 R2C 20K OHMS
R2 200K OHMS
R3 R6 R8 R17 R18 10K OHMS
R4 100 OHMS
R5 910 OHMS
R7 R9 R15 2.2K OHMS
R10 R11 R13 R16 1K OHMS
R12 5.6K OHMS
R14 R22 4.7K OHMS
R21 82K OHMS

	DATE	NAME
Orig.	23 · 12 · 63	N D J
Amend.	19 · 6 · 64	N D J
	6 · 7 · 64	N D J

TO ACCOMPANY RECORD No 1968/32

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. 682/3-104	SYNCHRONISATION COMPARATOR UNIT SA 1

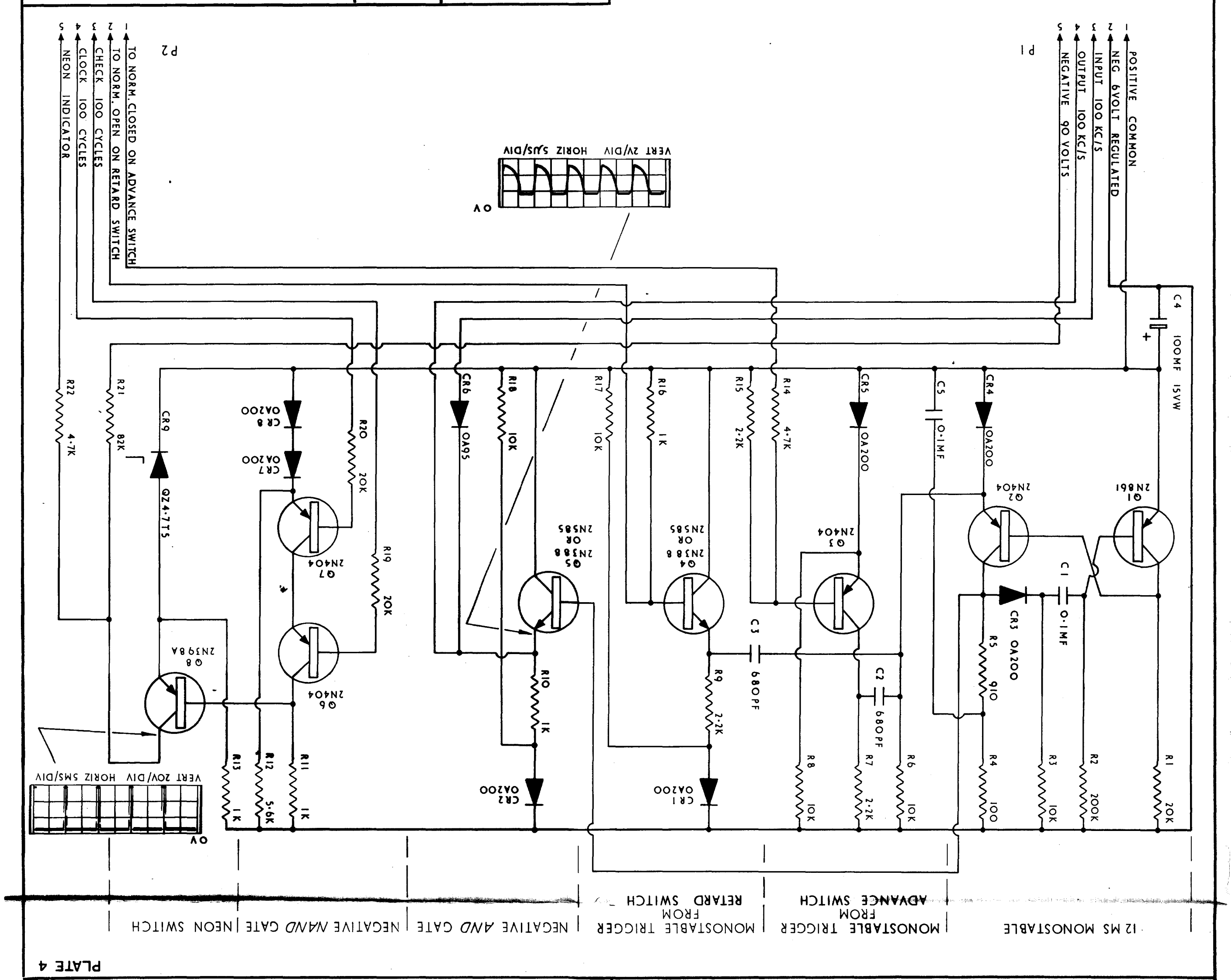


PLATE 4

COMPONENT LIST.

CONNECTORS.

P1 P2	SOURIAU 8140-02 MALE 5 PIN VOCAB. BKZ198

TRANSISTORS.

Q1 Q4 Q6	TRANSISTOR TYPE 2N861 VOCAB. BVT/2N861
Q2 Q5 Q7	TRANSISTOR TYPE 2N404 VOCAB. BVT/2N404
Q3 Q8	TRANSISTOR TYPE 2N388 or 2N585 VOCAB. BVT/2N388

DIODES.

CR1 CR2 CR3	SILICON DIODE TYPE OA200 VOCAB. BVD/OA200
CR4 CR5	GERMANIUM DIODE TYPE OA95 VOCAB. BVD/OA95

CAPACITORS.

C1	DUCON STYROSEAL TYPE DFB612 600VW 1000 PF VOCAB. BCP6102
C2	PHILIPS POLYESTER TYPE C296 125VW 0.01MFD VOCAB. BC01103
C3	PHILIPS POLYESTER TYPE C296 125VW 0.1MFD VOCAB. BC01104
C4 C5 C6	DUCON STYROSEAL TYPE DFB610 600VW 680PF VOCAB. BCP6681
C7	TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D 107x0015 100MFD 15VW

POTENTIOMETERS.

R14 R18 R19	BOURNS TRIMPOT TYPE 200L-1-503 50K OHMS Available ex PAINTON Australia. Melbourne.

RESISTORS.

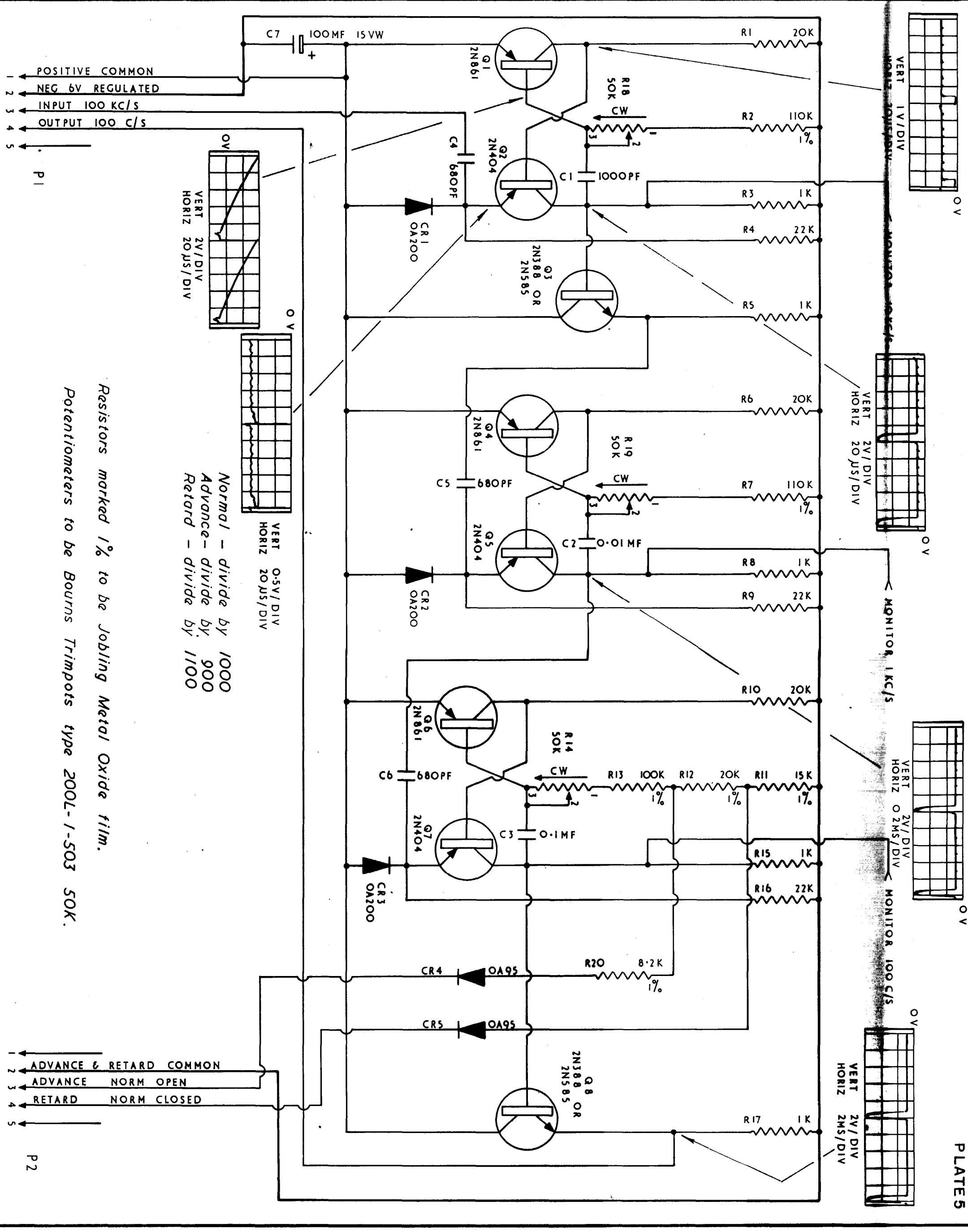
Following resistors to be WELWYN "METOX" ½ WATT TYPE F20

R1 R6 R10	20K OHMS
R3 R5 R8 R15 R17	1K OHMS
R4 R9 R16	22K OHMS

Following resistors to be JOBLING "ELECTROSIL" ½ WATT 1% TYPE N20

R2 R17	110K OHMS	VOCAB. BRB54114
R11	15K OHMS	VOCAB. BRB54153
R12	20K OHMS	VOCAB. BRB54203
R13	100K OHMS	VOCAB. BRB54104
R20	8.2K OHMS	VOCAB. BRB54822

	NAME	DATE
Orig.	N D J	23 · 12 · 63
Amend.	N D J	19 · 6 · 64



Resistors marked 1% to be Jobling Metal Oxide film.

Potentiometers to be Bourns Trimpots type 200L-1-503 50K.

Normal – divide by 1000
Advance – divide by 900
Retard – divide by 1100

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G82/3-105	MONOSTABLE FREQUENCY DIVIDER DV1

PLATE 5

TO ACCOMPANY RECORD No 1968/32

COMPONENT LIST.

CONNECTORS.

P1 P2 SOURIAU 8140-02 MALE 5 PIN
VOCAB. BKZ198

TRANSISTORS.

Q1 to Q8 TRANSISTOR TYPE 2N404
VOCAB. BVT/2N404

DIODES.

CR1 CR2 CR3 GERMANIUM DIODE TYPE OA95
CR4 CR5 CR6 VOCAB. BVD/OA95
CR7 CR8 GERMANIUM DIODE TYPE OA5
VOCAB. BVD/OA5

CAPACITORS.

C1 C2 DUCON STYROSEAL TYPE DF3608 600VW
470 PF VOCAB. BCP5471
C3 C6 PHILIPS POLYESTER TYPE C296 125VW
1 MFD VOCAB. BC01105
C4 C5 DUCON STYROSEAL TYPE DF3612 600VW
1000 PF VOCAB. BCP6102
C7 TANTALUM ELECTROLYTIC SPRAGUE TYPE
150D 107X0015 100 MFD 15VW
C8 TANTALUM ELECTROLYTIC SPRAGUE TYPE
150D 476X0015 47 MFD 15VW

RESISTORS.

Following resistors to be WELWYN "METOX" ½ WATT TYPE F20

R1 R2 2.2K OHMS
R3 180K OHMS
R4 R14 560 OHMS
R5 R6 R7 R8 R9 R11 10K OHMS
R10 R11 22K OHMS
R13 180K OHMS
R15 360 OHMS
R16 300 OHMS
R17 R18 1K OHMS

	DATE	NAME
Orig.	5 · 12 · 62	N D J
	9 · 4 · 63	N D J
Amend.	11 · 4 · 63	N D J
	6 · 8 · 63	N D J
	20 · 12 · 63	N D J
	19 · 6 · 64	N D J

TO ACCOMPANY RECORD No 1968/32

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS

Drawing No. 682/3-106

BISTABLE FREQUENCY DIVIDERS DV3/1 and DV3/2

P1/5 WITH RESPECT TO P1/4

VERT 0·5V/DIV HORIZ 5MS/DIV

VERT 2V/DIV HORIZ 5MS/DIV

P1 P2 1 2 3 4 5 50 C/S SIGNAL OUT

P1 1 POSITIVE 2 COMMON 3 REGULATED NEG 6 VOLTS 4 100 CYCLES INPUT 5 50 CYCLES OUT

C8 47MF 15 VW

C7 100MF 15VW

R16 300 R15 360

Q8 2N404 R14 560 CR8 OA5 R13 180K

Q5 2N404 C6 1 MF R18 1K

Q6 2N404 R12 10K

Q4 2N404 R9 10K C3 1MF R17 1K

Q3 2N404 CR7 OA5 R4 560 R3 180K

Q7 2N404 R2 2·2K

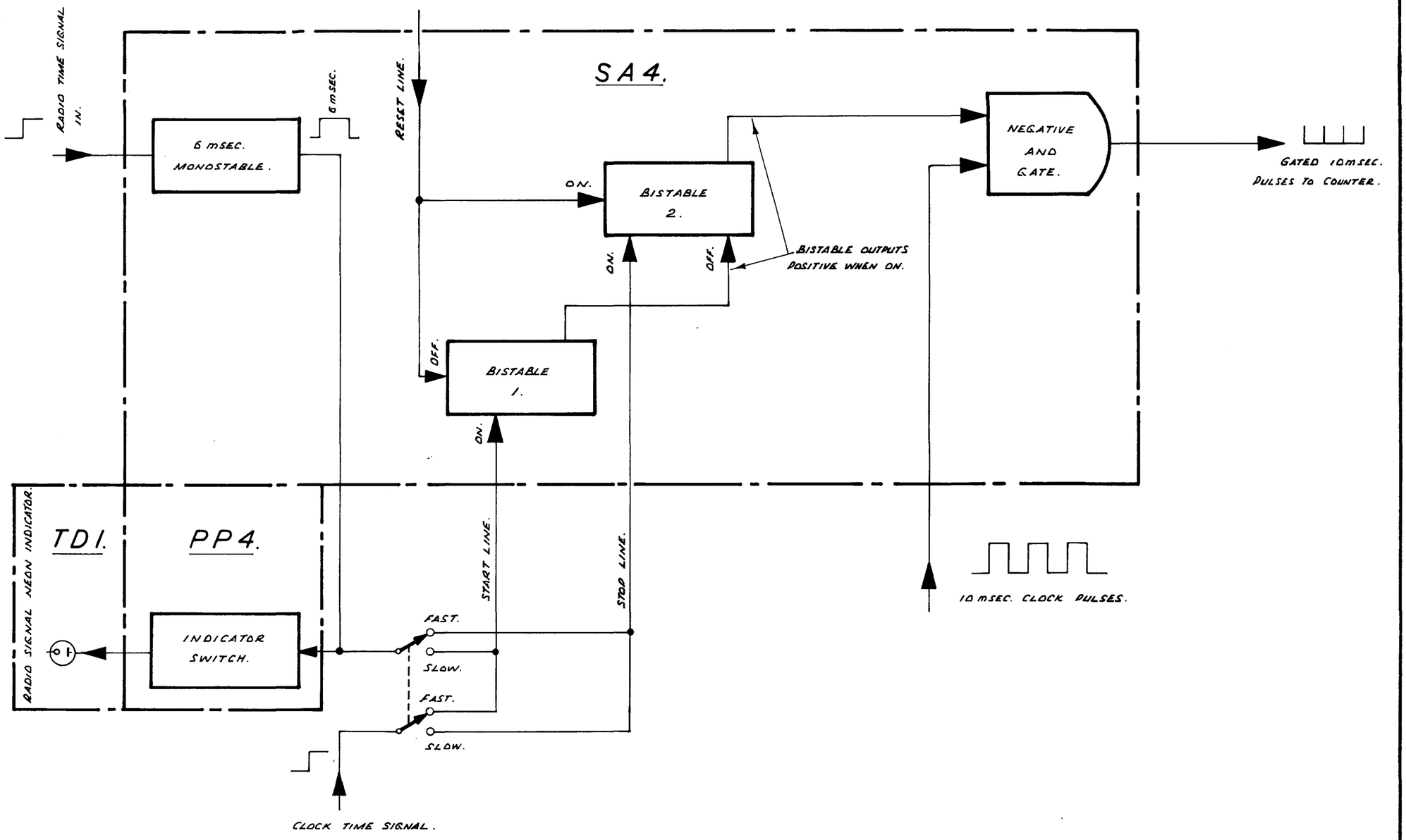
Q2 2N404 CR4 OA95 CR2 OA95 CR6 OA95 RB 10K C5 100PF R11 22K R6 10K C2 470PF

Q1 2N404 CR3 OA95 CR1 OA95 CR5 OA95 R10 22K C4 100PF R7 10K R5 10K C1 470PF R1 2·2K

PLATE 6

PLATE 7

	DATE	NAME
Orig.	2-7-64.	R. G. AN.
Amend.		



TO ACCOMPANY RECORD No 1968/32

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G82/3-107	TIME COMPARATOR UNIT BLOCK DIAGRAM

COMPONENT LIST.

CONNECTORS.

P1 P2	SOURIAU 8140-02 MALE 5 PIN VOCAB. BKZ198

TRANSISTORS.

Q1 Q2 Q3 Q4 Q8	TRANSISTOR TYPE 2N404 VOCAB. BVT/2N404
Q5 Q6	TRANSISTOR TYPE 2N388 VOCAB. BVT/2N388
Q7	TRANSISTOR TYPE 2N861 VOCAB. BVT/2N861

DIODES.

CR1 CR2 CR3	GERMANIUM DIODE TYPE OA95 VOCAB. BVD/OA95
CR4 CR5	SILICON DIODE TYPE OA200 VOCAB. BVD/OA200

CAPACITORS.

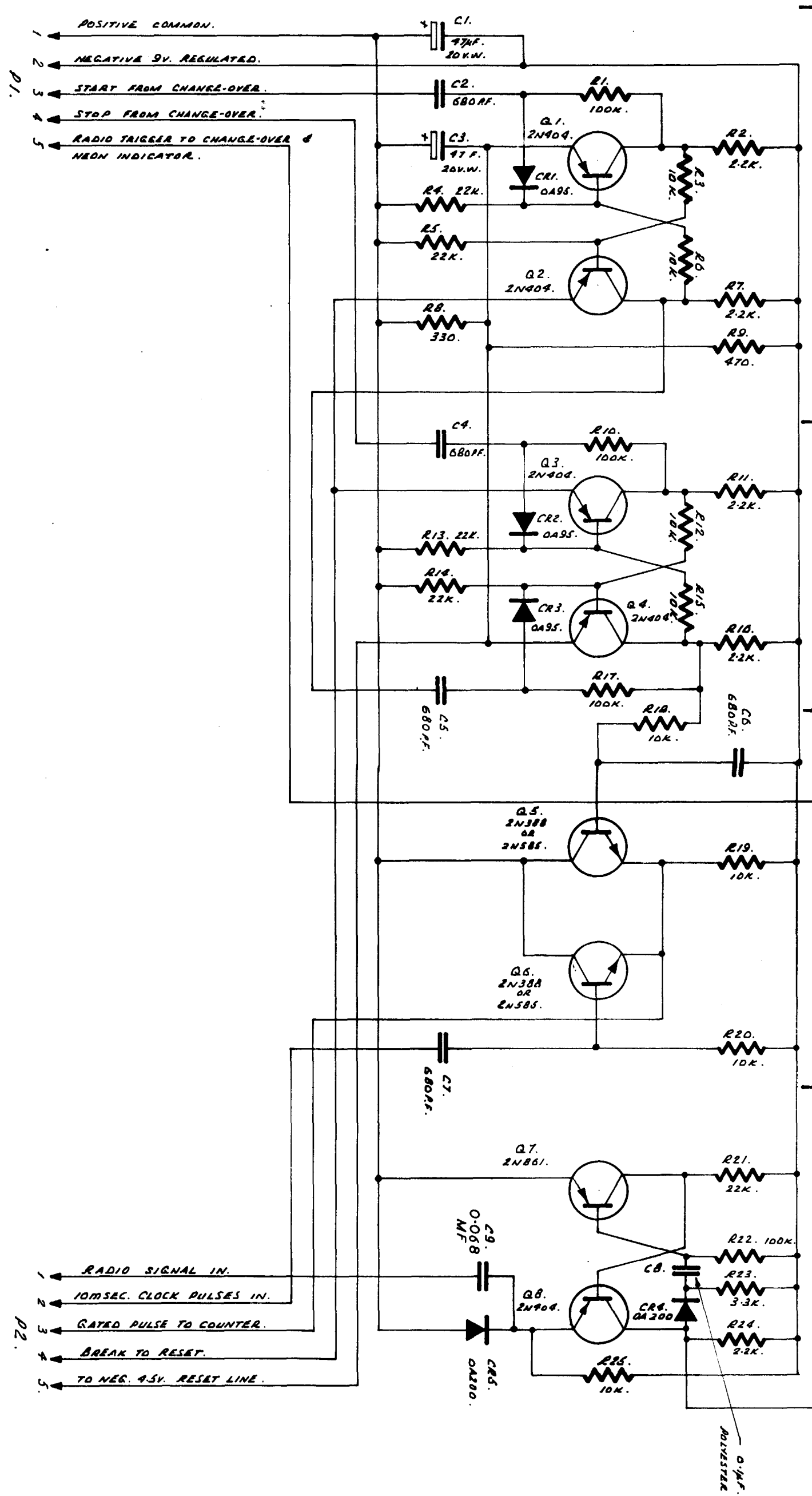
C1 C3	TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D 476x0020 47 MFD 20VW
C2 C4 C5	DUCON STYROSEAL TYPE DFB610 600VW
C6 C7	680 PF VOCAB. BCP6681
C8	PHILIPS POLYESTER TYPE C296 125VW 0.1 MFD VOCAB. BC01104
C9	PHILIPS POLYESTER TYPE C296 125VW 0.068 MFD VOCAB. BC01683

RESISTORS.

Following resistors to be WELWYN "METOX" ½ WATT TYPE F20

R1 R10 R17 R22	100K OHMS
R2 R7 R11 R16 R24	2.2K OHMS
R3 R6 R12 R15 R18 R19 R20 R25	10K OHMS
R4 R5 R13 R14 R21	22K OHMS
R8	330 OHMS
R9	470 OHMS
R23	3.3K OHMS

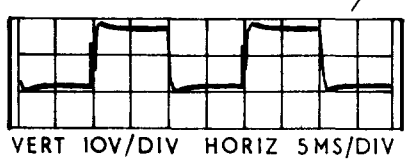
	NAME	DATE
Orig.	R. CAW.	6-7-64.
Amend.	N D J	30 · 7 · 64
REDRAWN.	N D J	5 · 8 · 64

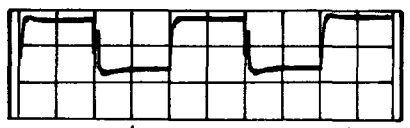


BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G82/3-108
TIME COMPARATOR UNIT SA4	PLATE 8

TO ACCOMPANY RECORD No 1968/32

	DATE	NAME
Orig.	5 · 12 · 62	N D J
Amend.	10 · 4 · 63	N D J
	7 · 8 · 63	N D J
	20 · 12 · 63	N D J
	22 · 6 · 64	N D J





COMPONENT LIST.

CONNECTORS.
P1 P2 SOURIAU 3140-02 MALE 5 PIN
VOCAB. BX2193

TRANSISTORS.
Q1 Q2 TRANSISTOR TYPE 2N301A
VOCAB. BVT/2N301A

DIODE.
CR1 SILICON RECTIFIER TYPE 5A4

VOLTAGE DEPENDENT RESISTOR.
R1 PHILIPS VDR TYPE E299DG/P224

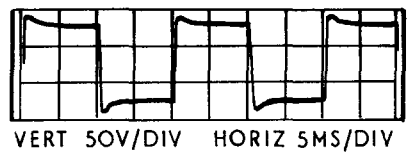
TRANSFORMER.
T1

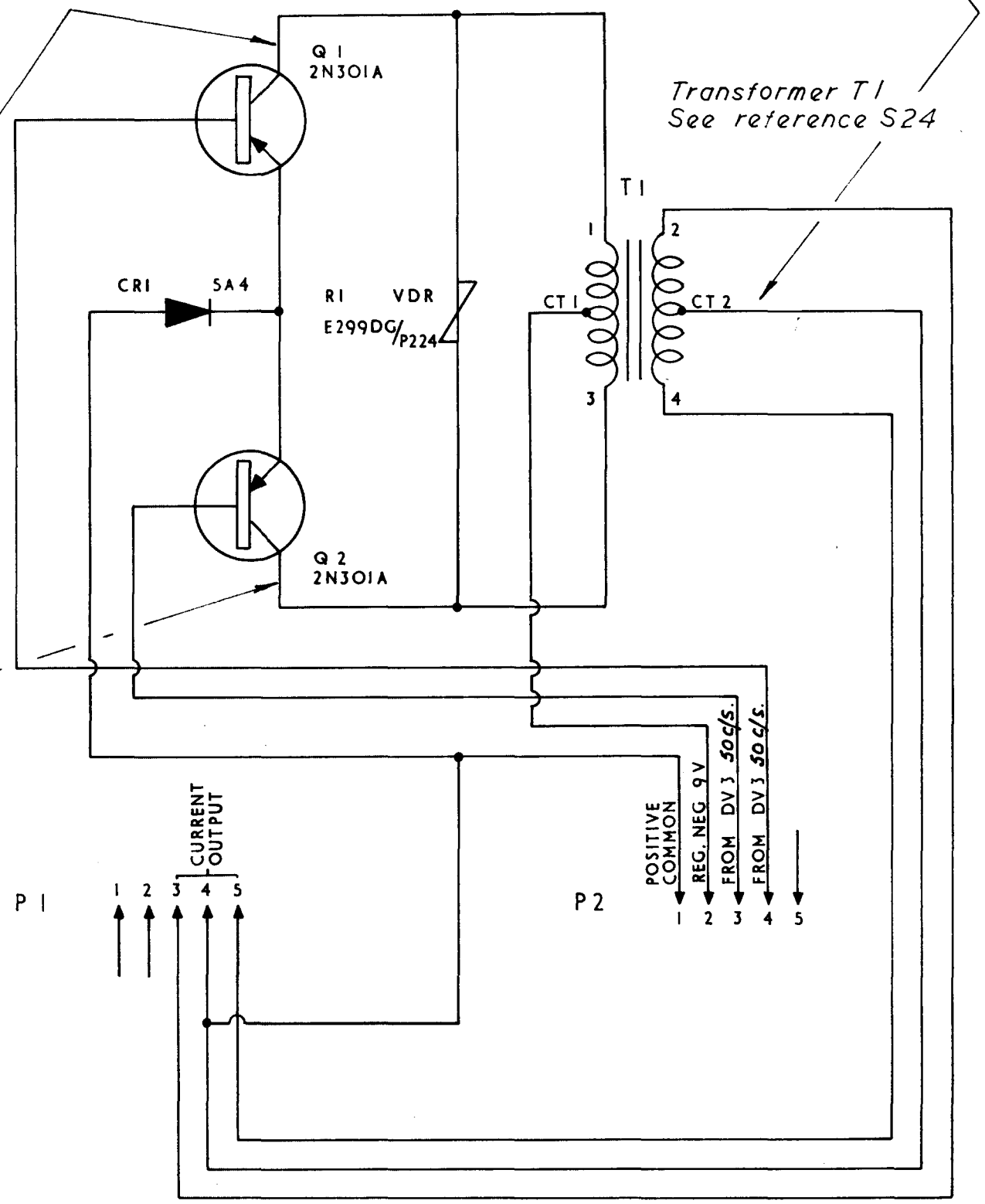
CORE. ENGLISH ELECTRIC TYPE HWR 10/8/5
½ Primary 200 turns No.24 B & S double s
½ Secondary 750 turns No.29 B & S double
Fit one layer 0.002" paper between prima
Both primary and secondary to be Bifilar wound.

Reference. S24

PLATE 9

TI TOTAL SECONDARY





BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G82/3-109	POWER AMPLIFIER AMI

TO ACCOMPANY RECORD No 1968/32

COMPONENT LIST.

CONNECTORS.

P1	SOURIAU 8140-02 MALE 5 PIN VOCAB. BKZ198
P2	SOURIAU 8140-07 MALE 3 PIN

TRANSISTORS.

Q1 Q2	TRANSISTOR TYPE 2N301A VOCAB. BVT/2N301A

DIODE.

CR1	SILICON RECTIFIER TYPE 5A4

VOLTAGE DEPENDENT RESISTOR.

R1	PHILIPS VDR TYPE E299DG/P228

TRANSFORMER.

T1	CORE. ENGLISH ELECTRIC TYPE HWR 10/12/13 ½ Primary 300 turns No.25 B & S double solderite wire. ½ Secondary 45 turns No.18 B & S double solderite wire. Fit one layer 0.002" paper between primary and secondary. Both primary and secondary to be bifilar wound. Reference. W69

Orig.

Amend.

NAME	DATE
N D J	9 · 4 · 63
N D J	11 · 4 · 63
N D J	20 · 12 · 63
N D J	22 · 6 · 64

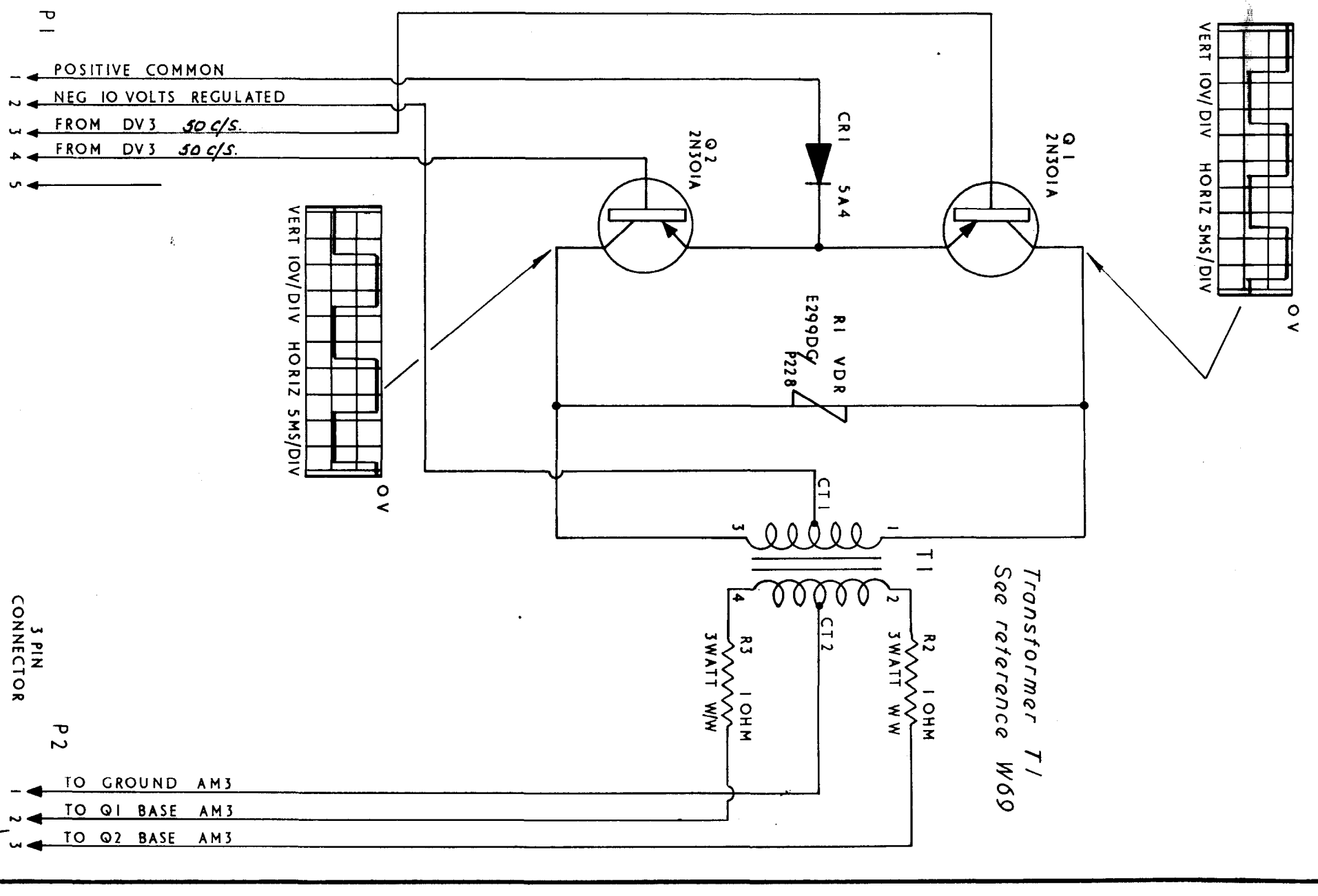


PLATE 10

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS

Drawing No. G82/3-110

POWER AMPLIFIER AM2

TO ACCOMPANY RECORD No 1968/32

COMPONENT LIST.

CONNECTORS.
P1 P2A P2B — SOURIAU 8140-07 MALE 3 PIN

TRANSISTORS.
Q1 Q2 — TRANSISTOR TYPE 2N174
VOCAB. BVT/2N174

CAPACITOR.
C1 — TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D
157x0015 150MFD 15VW

VOLTAGE DEPENDENT RESISTOR.
R1 — PHILIPS TYPE E299DG/P228

R2 — PHILIPS TYPE E299DE/P350

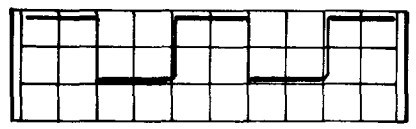
TRANSFORMER T1.
CORE. ENGLISH ELECTRIC TYPE HWR 40/12/13. FORMER No.5/8983. CASE SHROUDED CLAMP No.54/2759.
½ Primary. 78 turns No.16 B & S double solderite wire. Bifilar wound. Wind to nearest full layer.
(Approx. 77 turns.)

Secondary. 2300 turns No.26 B & S double solderite wire. Fit 0.005" pressphan between primary and secondary.

Insulate with Silicon varnish type MS994 with catalyst LS15.

Reference. S22. Serial No.5

	DATE	NAME
Orig.	16 · 4 · 63	N D J
Amend.	21 · 12 · 63	N D J
	23 · 6 · 64	N D J



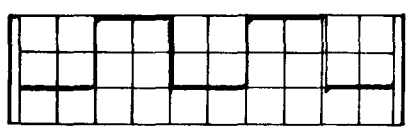
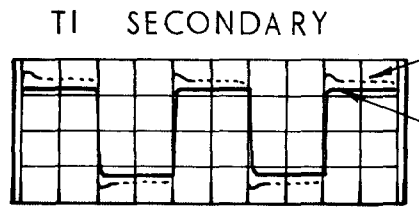
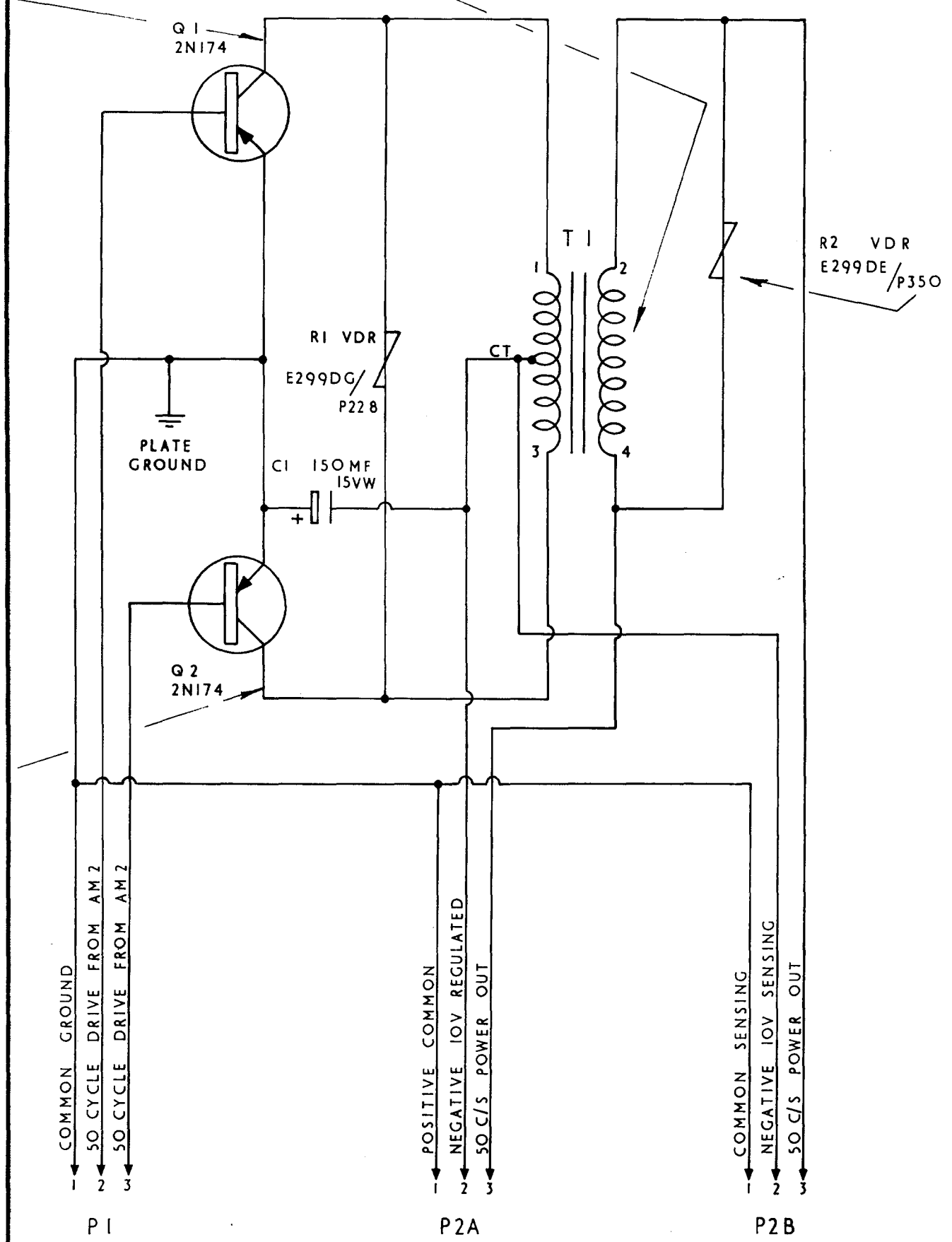


PLATE II



Transformer T1. Reference S22.



All connectors 3 pin

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G82/3-111	POWER AMPLIFIER AM3

TO ACCOMPANY RECORD No 1968/32

COMPONENT LIST. Following list comprises electronic components only. For parts list of mechanical assembly refer to clock drawings book No.2.

CONNECTORS.

P2 P3 P4	SOURIAU 8140-02 MALE 5 PIN VOCAB. BKZ198

PHOTO-TRANSISTORS.

Q1 Q2 Q3 Q4	PHOTO-TRANSISTOR TYPE OCP71

RESISTORS.

R1 R2 R3 R4	PHILIPS NTC TYPE B832007P/4K7 4.7K OHMS VOCAB. BRZO 1472

LAMPS.

DS1 DS2 DS3	THORN ATLAS SUB-MIN. TYPE L1012
DS4	For holder refer drawing No.D33/D44 book No.2
DS5	THORN ATLAS SUB-MIN. TYPE L1015 c/w HOLDER TYPE THORN ATLAS 80/10/2348/clear.

CAPACITORS.

C1 C2 C3 C4	PHILIPS POLYESTER TYPE C296 125VW 1 MFD VOCAB. BC01105

MOTOR.

B1	PHILIPS SYNCHRONOUS TYPE AU5020/94

CHOKE.

L1	INDUCTANCE 5 HENRIES. RESISTANCE 450 OHM Choke made from Rola speaker transformer type E1, with secondary removed and air gap increased to 0.005"

SWITCH.

S1	CUTLER HAMMER TOGGLE SWITCH TYPE 8372 K8 DP.ST Vocab. BST13

Add following resistors.

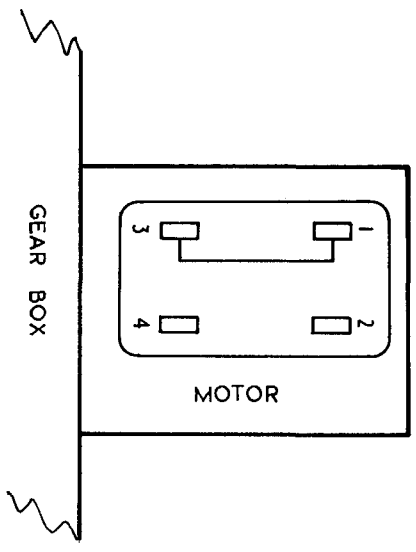
R5 R6 R7 R8	Welwyn "Metox" ½ WATT TYPE F20 22 OHMS Vocab. BRB56220

Amend.	DATE	NAME
Orig.	25-5-64.	R. G.W.
	29-6-64	N D J
	12-8-65	N D J
	22-11-65	N D J

MOTOR SWITCH S1 ADDED. THIS MOD MADE TO ONE UNIT ONLY THIS DATE. REPLACES CLUTCH.

RESISTORS R5-8 ADDED

MOTOR CONNECTIONS



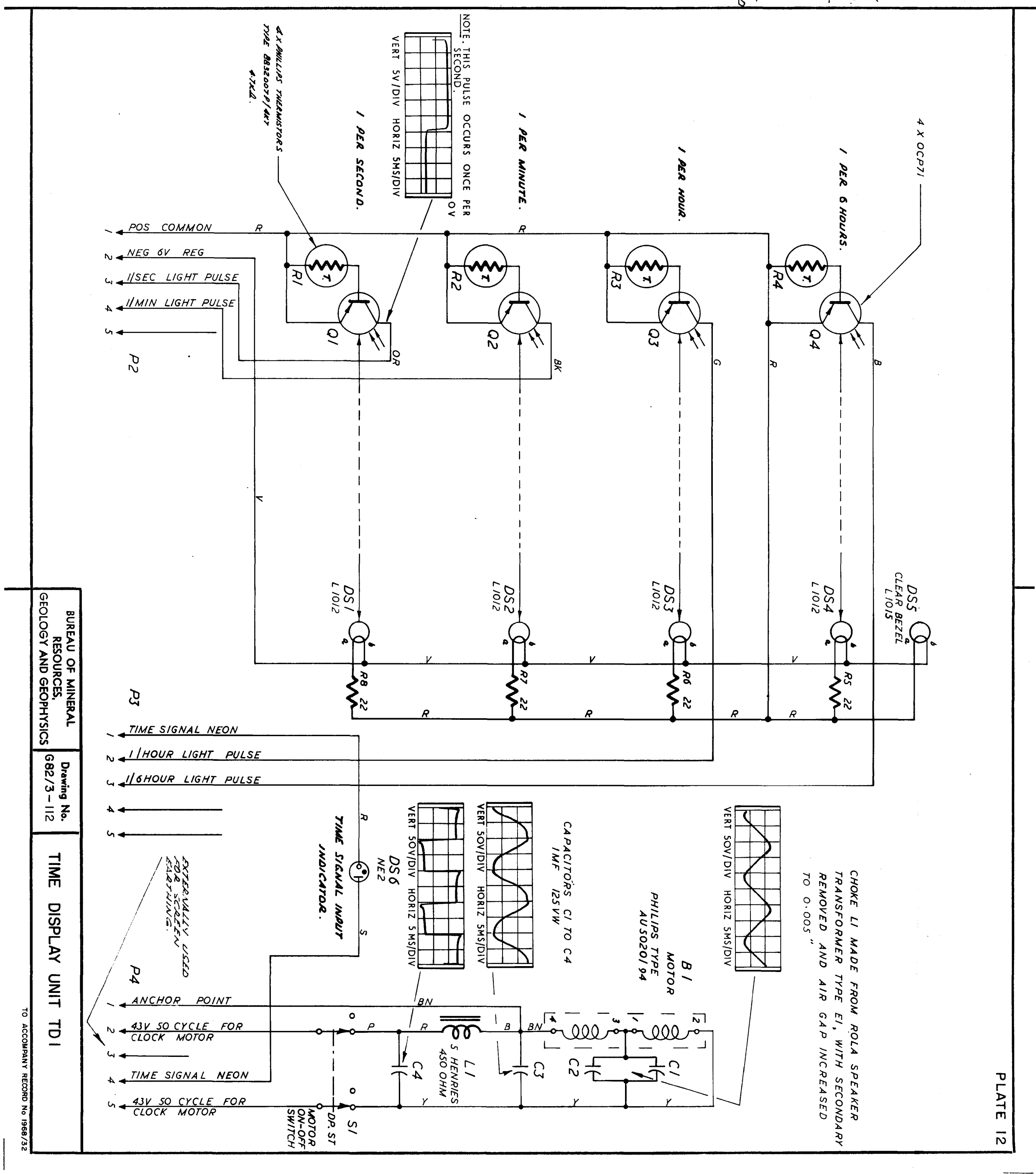


PLATE 12

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS

Drawing No. G82/3-112

TIME DISPLAY UNIT TD1

TO ACCOMPANY RECORD No 1968/32

COMPONENT LIST.

CONNECTORS.

P1 P2	SOURIAU 8140-02 MALE 5 PIN VOCAB. BKZ199

TRANSISTORS.

Q1 Q5 Q8 Q10	PHOTO TRANSISTOR TYPE OCP71
Q2 Q3 Q4 Q6 Q7 Q9 Q11 Q14	TRANSISTOR TYPE 2N404 VOCAB. BVT2N404
Q12	TRANSISTOR TYPE 2N388 VOCAB. BVT/2N388
Q13	TRANSISTOR TYPE 2N861 VOCAB. BVT/2N861
Q15	TRANSISTOR TYPE T2309

DIODES.

CR1 CR3 CR4 CR6 CR10	GERMANIUM DIODE TYPE OA95 VOCAB. BVD/OA95
CR2 CR5 CR7 CR8 CR9 CR11	SILICON DIODE TYPE OA200 VOCAB. BVD/OA200

CAPACITORS.

C1	TANTALUM SPRAGUE TYPE ELECTROLYTIC 150D 107x0015 100MFD 15VW
C2	PHILIPS POLYESTER TYPE C296 125VW 0.22MFD VOCAB. BC01224
C3	PHILIPS POLYESTER TYPE C296 125VW 0.1MFD VOCAB. BC01104
C4	DUCON STYROSEAL TYPE DFB610 500VW 680 PF VOCAB. BCP5681

RESISTORS.

Following resistors to be WELWYN "METOX" ½ WATT TYPE F2C

R2 R4 R8 R11 R15 R19 R23	4.7K OHMS
R3 R5 R9 R12 R16 R20	47K OHMS
R21	20K OHMS
R22	200K OHMS
R24	100 OHMS
R25	10K OHMS
R28	910 OHMS

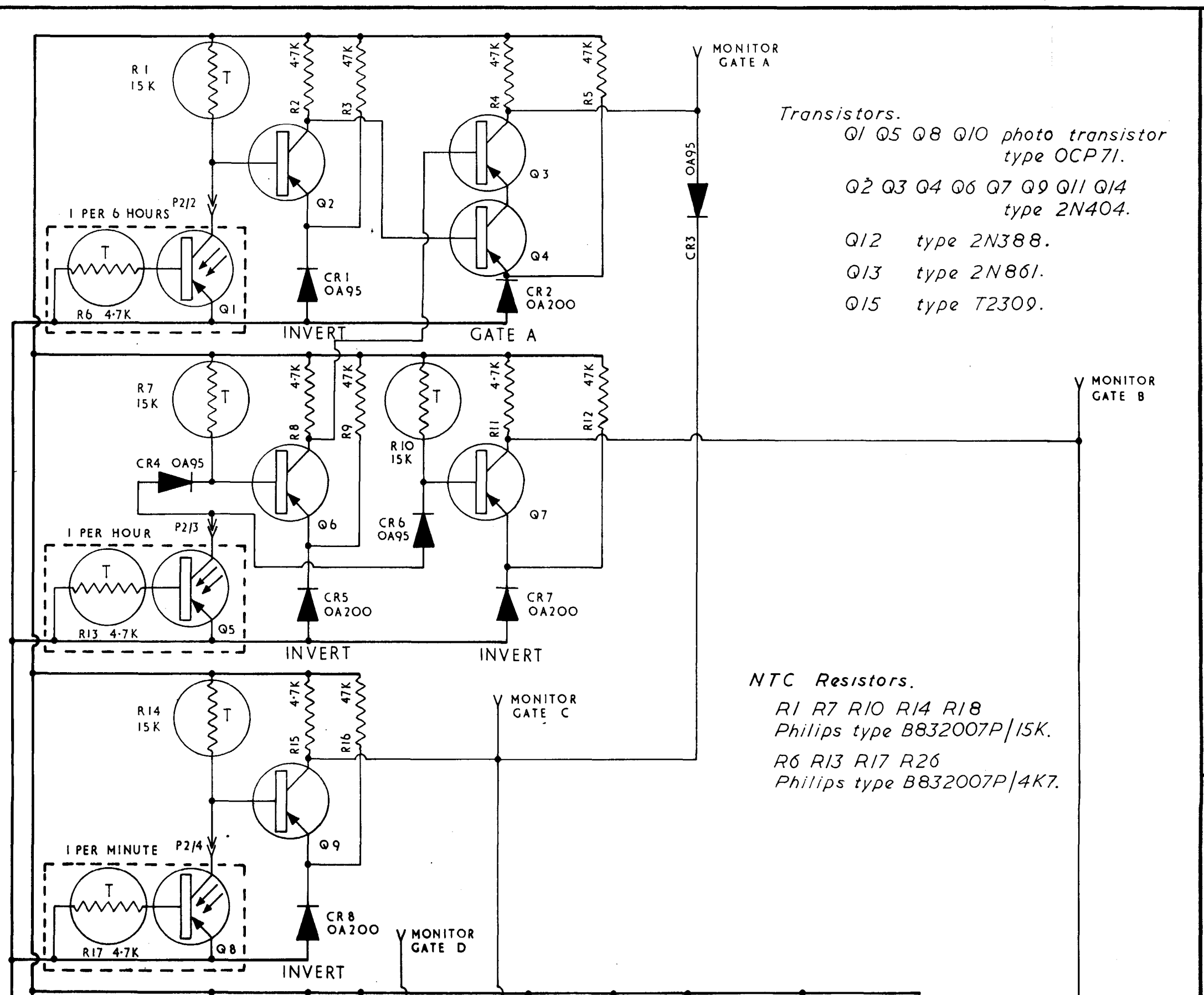
POTENTIOMETER.

R27	BOURNS TRIMPOT TYPE 200L-1-503 Available ex PAINTON Australia. Melbourne.	50K OHMS

N.T.C Resistors.

R1 R7 R10 R14 R18	PHILIPS TYPE B8 32007P/15K VOCAB. BRZ01153	15K OHMS
R6 R13 R17 R26	PHILIPS TYPE B8 32007P/4K7 VOCAB. BRZ01472	4.7K OHMS

	DATE	NAME
Orig.	13 · 8 · 63	N D J
Amend.	20 · 12 · 63	N D J
	19 · 6 · 64	N D J
	2 · 7 · 64	N D J



Transistors.

Q1 Q5 Q8 Q10 photo transistor type OCP71.

Q2 Q3 Q4 Q6 Q7 Q9 Q11 Q14 type 2N404.

Q12 type 2N388.

Q13 type 2N861.

Q15 type T2309.

NTC Resistors.

R1 R7 R10 R14 R18
Philips type B832007P/15K.

R6 R13 R17 R26
Philips type B832007P/4K7.

Indicates mounted on TD 1

TO ACCOMPANY RECORD No 1968/32

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS

Drawing No. G82/3-113

LIGHT-GATE and 1-SECOND MONOSTABLE CIRCUITS, SA2

PLATE 13

COMPONENT LIST.

CONNECTORS.

P1 P2A P2B	SOURIAU 8140-02 MALE 5 PIN VOCAB. BKZ198

TRANSISTORS.

Q1 Q4	TRANSISTOR TYPE 2N861 VOCAB. BVT/2N861
Q2 Q5	TRANSISTOR TYPE 2N404 VOCAB. BVT/2N404
Q3 Q6	TRANSISTOR TYPE T2309

DIODES.

CR1 CR3 CR4 CR6 CR7 CR8 CR9 CR10	GERMANIUM DIODE TYPE OA95 VOCAB. BVD/OA95
CR2 CR5	SILICON DIODE TYPE OA200 VOCAB. BVD/OA200

CAPACITORS.

C1	TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D 336x0015 33MFD 15VW
C2 C5	PHILIPS POLYESTER TYPE C296 125VW 0.1 MFD VOCAB. BC01104
C3 C6	DUCON STYROSEAL TYPE DFB610 600VW 680 PF VOCAB. BCP6681
C4	TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D 156x0015 15MFD 15VW
C7	TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D 107x0015 100MFD 15VW

RESISTORS.

Following resistors to be WELWYN "METOX" ½ WATT TYPE F20

R1 R8	20K OHMS
R2	150K OHMS
R3 R10	4.7K OHMS
R4 R11	100 OHMS
R5 R12	10K OHMS
R7 R14	910 OHMS
R9	160K OHMS

POTENTIOMETERS.

R6 R13	BOURNS TRIMPOT TYPE 200L-1-503 50K OHMS Available ex PAINTON Australia. Melbourne.

RELAYS.

A.B.C	SIEMENS HALSKE HERMETICALLY SEALED TYPE TRLS 162A TBV65416/1100. C/W SOCKETS TYPE TSTV24D AND MOUNTING BRACKETS TYPE TSTV24 T8.

	Amend.	Orig.
DATE	22 · 6 · 64	9 · 8 · 63
NAME	N D J	N D J

I PER MINUTE MONOSTABLE DURATION 2 SECONDS

I PER HOUR MONOSTABLE DURATION 4 SECONDS

P1

POSITIVE COMMON
NEG 6V REGULATED
FROM EMIT. FOLLOWER ON 1/SEC. MONOSTABLE
TO GATE B
TO GATE C

C7 100MF 15VW

Relays A B and C. Siemens Halske hermetically sealed type Trls 162A Tbv 65416/1190

Screens

P2A

BREAK 1/SECOND
BREAK 1/SECOND
MAKE 1/SECOND
MAKE 1/SECOND

P2B

CLOCK 1/SEC PULSE OUT TO CHANGEOVER SWITCH
MAKE 1/MINUTE
MAKE 1/MINUTE
MAKE 1/HOUR
MAKE 1/HOUR

Q4 2N861 — R8 20K — R13 50K — R9 160K — C4 15MF 15VW — R10 4·7K — Q5 2N404 — CR4 OA95 — R14 910 — R11 100 — CR5 OA200 — C5 0·1MF — R12 10K — Q6 T2309 — C6 680 PF — CR6 OA95 — B/2 130 — 1/MINUTE RELAY — CR7 OA95 — Y MONITOR GATE C

Q1 2N861 — R1 20K — R6 50K — R2 150K — C1 33MF 15VW — R3 4·7K — Q2 2N404 — CR1 OA95 — R7 910 — R4 100 — CR2 OA200 — C2 0·1MF — R5 10K — Q3 T2309 — C3 680PF — A/2 130 — 1/HOUR RELAY — CR3 OA95 — Y MONITOR GATE B

R15 1K — CR10 OA95 — C/2 130 — 1/SECOND RELAY — CR8 OA95 — CR9 OA95

C1 NORM. CLOSED 5 6 7

C2 NORM OPEN 9 10 8

B2 NORM. OPEN 9 10 8

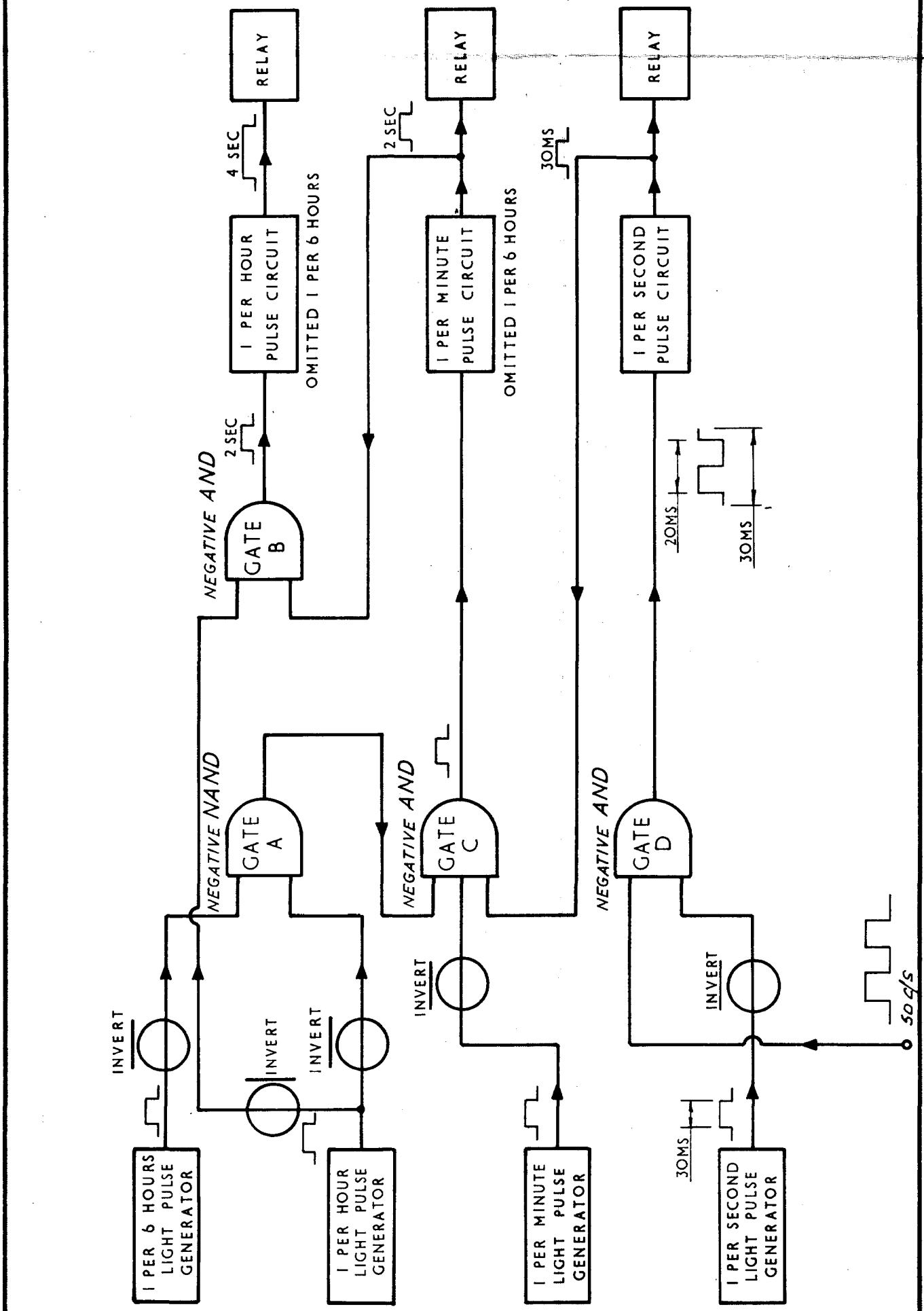
A2 NORM. OPEN 9 10 8

PLATE 14

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G82/3-114
1-MINUTE and 1-HOUR MONOSTABLE CIRCUITS and TIMING RELAYS, SA3	TO ACCOMPANY RECORD No 1968/32

	DATE	NAME
Orig.	13 · 8 · 63	N D J
Amend.	20 · 12 · 63	N D J
	29 · 6 · 64	N D J

PLATE 15



NCD 2

BLOCK DIAGRAM

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G82/3-115	SA2 and SA3 BLOCK DIAGRAM

TO ACCOMPANY RECORD No 1968/32

COMPONENT LIST.

CONNECTORS.
P1 P2 SOURIAU 8140-02 MALE 5 PIN
VOCAB. BKZ198

TRANSISTORS.
Q1 to Q8 TRANSISTOR TYPE 2N404
VOCAB. BVT/2N404

DIODES.
CR1 to CR14 GERMANIUM DIODE TYPE OA95
VOCAB. BVD/OA95

CAPACITORS.
C1 to C8 DELETED.
C9 C10 C11 C12 DUCON STYROSEAL TYPE DPB610 600VW
C13 C14 C15 C16 680PF VOCAB. BCP6681
C17 C18 TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D 476x0020 47MFD 20VW

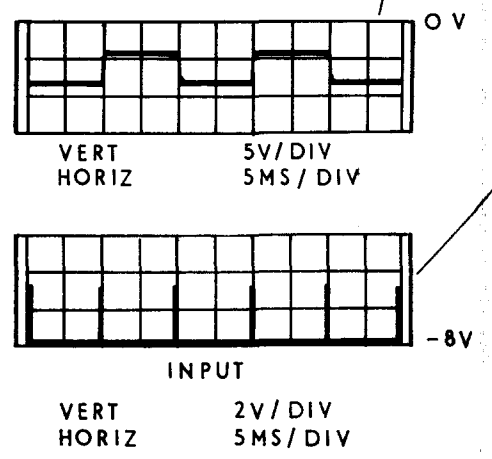
RESISTORS.
Following resistors to be WELWYN "METOX" ½ WATT TYPE F20

R1 R4 R6 R8	2.2K OHMS
R2 R3 R5 R7 R9 R40 R41 R42 R43	4.7K OHMS
R10 R11 R12 R13 R14 R15 R16 R17	10K OHMS
R18 R19 R20 R21 R22 R23 R24 R25	22K OHMS
R26 R27 R28 R29 R30 R31 R32 R33	100K OHMS

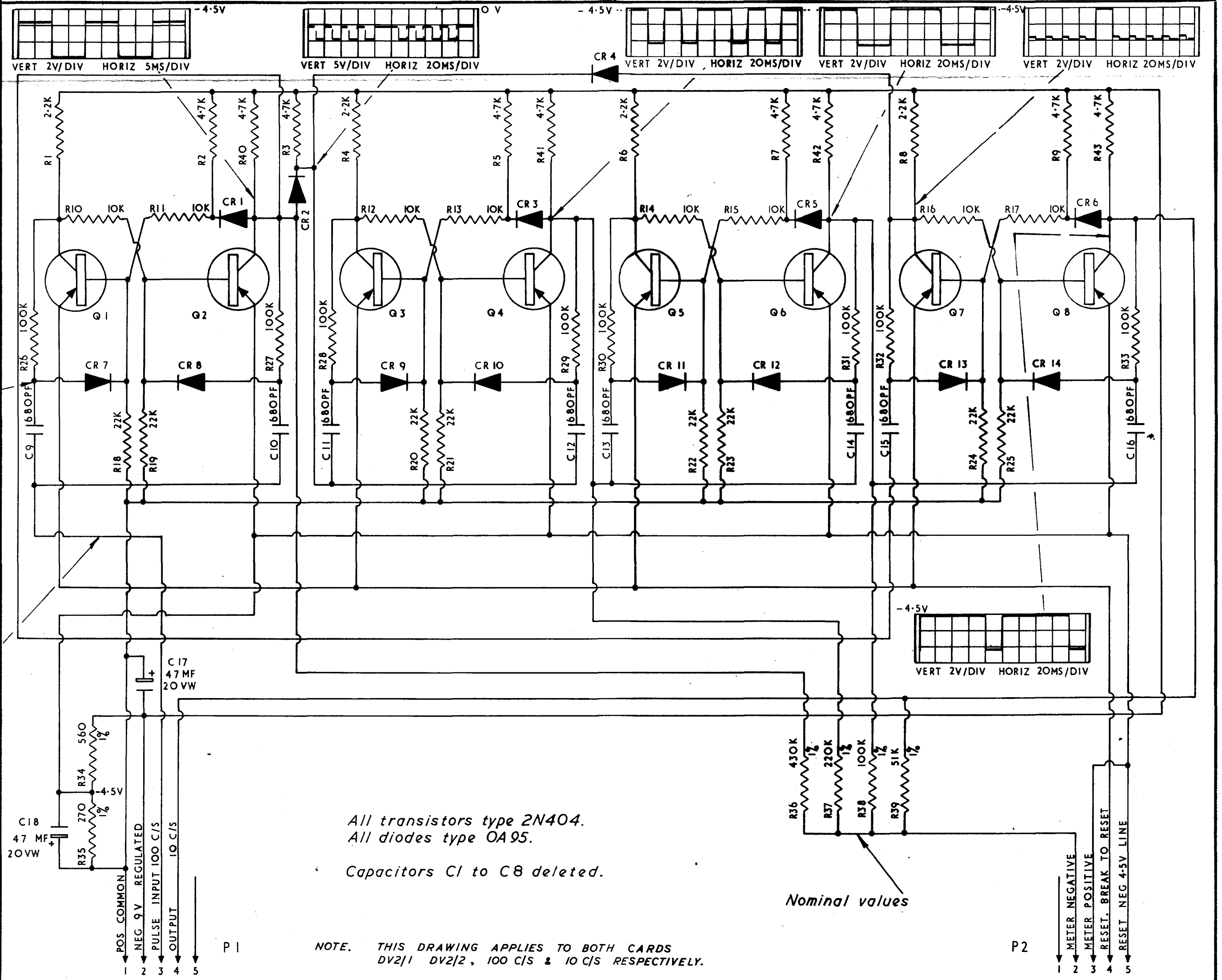
Following resistors to be JOBLING "ELECTROSIL" ¼ WATT 1% TYPE N20

R34	560 OHMS	VOCAB. BRB54561
R35	270 OHMS	VOCAB. BRB54271
R36	430K OHMS	VOCAB. BRB54434
R37	220K OHMS	VOCAB. BRB54224
R38	100K OHMS	VOCAB. BRB54104
R39	51K OHMS	VOCAB. BRB54513

	DATE	NAME
Orig.	25 · 3 · 63	N D J
Amend.	6 · 8 · 63	N D J
	20 · 12 · 63	N D J
	19 · 6 · 64	N D J



To observe waveforms on DV2/2 multiply time base by 10.



All transistors type 2N404.
All diodes type OA95.

Capacitors C1 to C8 deleted.

Nominal values

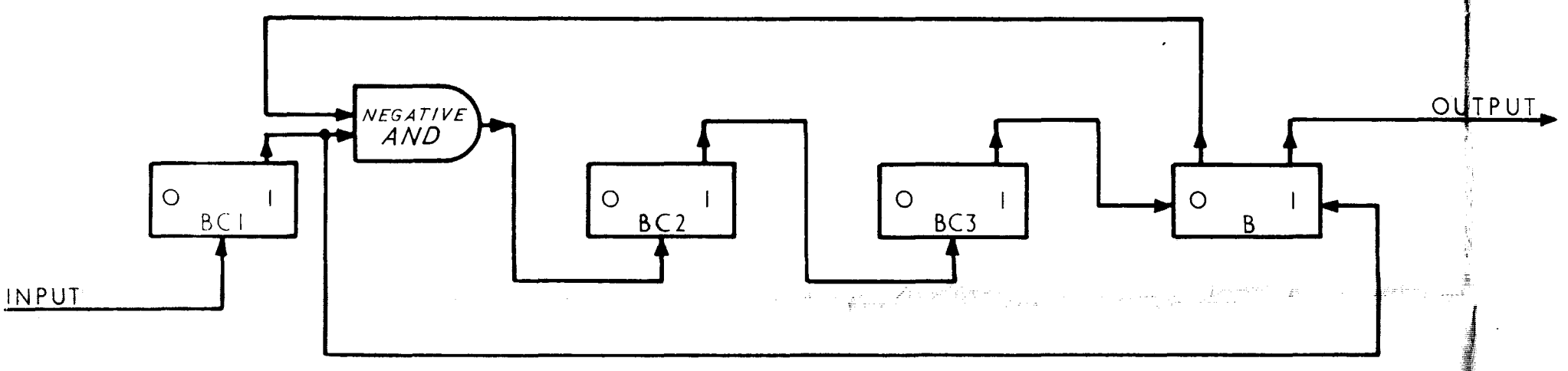
NOTE. THIS DRAWING APPLIES TO BOTH CARDS DV2/1 DV2/2, 100 C/S & 10 C/S RESPECTIVELY.

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G82/3-116	DECADE FREQUENCY DIVIDERS DV2

TO ACCOMPANY RECORD No 1968/32

	NAME	DATE
Orig.	N D J	13 · 3 · 63
Amend.	N D J	7 · 7 · 64

① LOGICAL OPERATION



NOTES. (a) BC = BINARY COUNTER

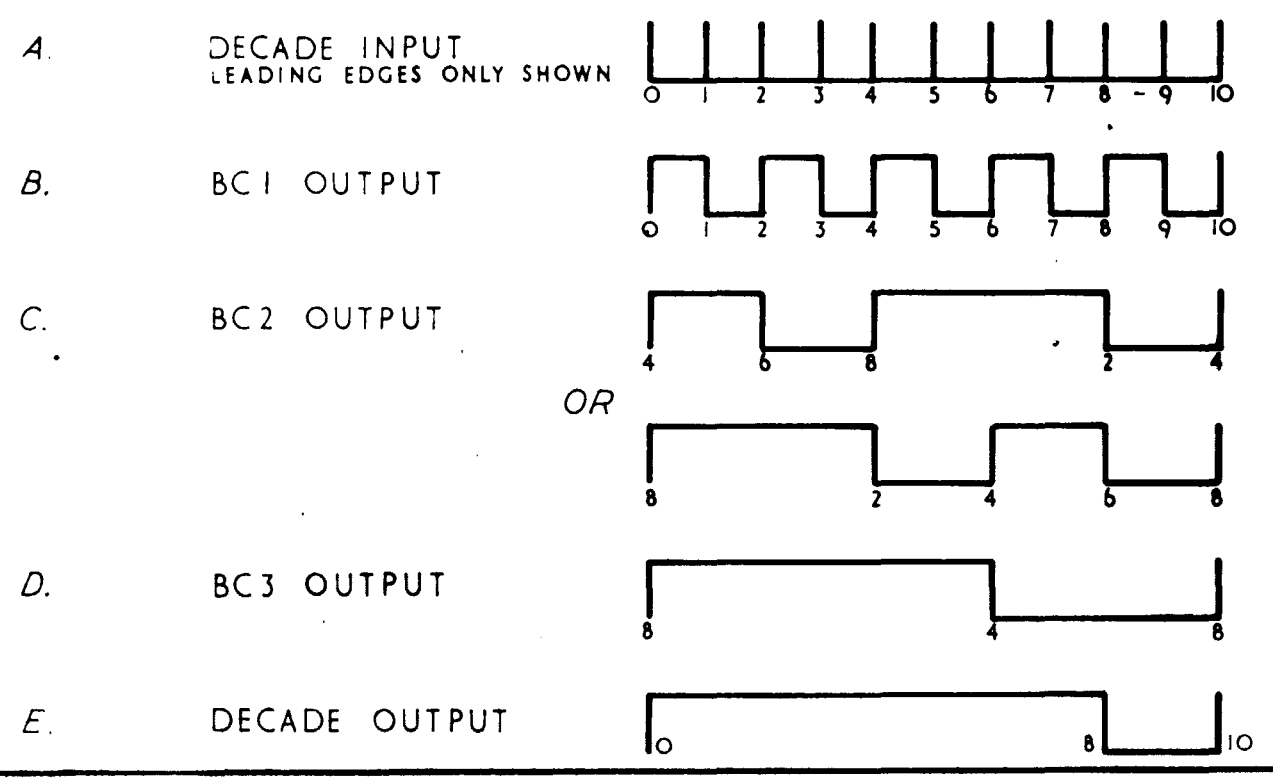
(b) B = BISTABLE — A "true" (e.g. positive) signal at the 0 input produces a "true" signal at the 0 output. Similarly, a "true" signal at the 1 input produces a "true" signal at the 1 output. This is purely a logical representation. If the 0 input of an actual transistor bistable is at the base of transistor No.1, the 0 output is at the collector of transistor No.2.

(c) Denoting a "true" output by 1, and a "false" output by 0, the following table indicates the dividing sequence.

Input pulse No.	Output BC1	Output BC2	Output BC3	Output B
0	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	0	0	1	1
4	1	1	0	1
5	0	1	0	1
6	1	0	0	1
7	0	0	0	1
8	1	1	1	0
9	0	1	1	0
10	1	1	1	1

② WAVEFORMS

The following waveforms should be observed when triggering the C.R.O with a positive going signal. Horizontal axes are calibrated in multiples of the decade input signal period.



Both waveforms will appear simultaneously, as the C.R.O cannot distinguish between leading edges at 4 and 8.

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS

Drawing No. G82/3-117

DECADE FREQUENCY DIVIDERS DV2, OPERATION AND WAVEFORMS

TO ACCOMPANY RECORD No 1968/32

PLATE 17

COMPONENT LIST.

CONNECTORS.

P1 P2	SOURIAU 8140-02 MALE 5 PIN VOCAB. BKZ198

TRANSISTORS.

Q1	TRANSISTOR TYPE T2309
Q2	TRANSISTOR TYPE OC22 VOCAB. BVT/OC22 Mounted on rear panel.
Q3 Q6	TRANSISTOR TYPE 2N404 VOCAB. BVT/2N404
Q4	TRANSISTOR TYPE 2N388 VOCAB. BVT/2N388
Q5	TRANSISTOR TYPE 2N861 VOCAB. BVT/2N861

DIODES.

CR1	SILICON ZENER DIODE TYPE QZ4.7T5 VOCAB. BVD/QZ4.7T5
CR2	SILICON DIODE TYPE OA200 VOCAB. BVD/OA200
CR3	SILICON ZENER DIODE TYPE QZ5.1T5 VOCAB. BVD/QZ5.1T5

CAPACITORS.

C1	TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D 106x0020 10MFD 20VW
C2	TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D 686x0015 68MFD 15VW

RESISTORS.

Following resistors to be WELWYN "METOX" TYPE F20 ½ WATT

R1 R2 R4	2.2K OHMS
R5	20 OHMS
R6 R11	47 OHMS
R8	2.7K OHMS
R9	4.7K OHMS
R10	470 OHMS

POTENTIOMETER.

R7	BOURNS TRIMPOT TYPE 200L-1-101 100 OHMS Available ex PAINTON Australia. Melbourne.

Following resistors to be WELWYN type AW3101 3 WATT W/W

R3 R3A	1 OHM. (Nominal)

	DATE	NAME
Orig.	30 · 12 · 63	N D J
Amend.	19 · 6 · 64	N D J

Note. Resistor R3 nominally 1 ohm Welwyn wire wound, but should be padded to adjust cutout within range 700 to 900 milliamps at AMBIENT AND 60°C.

Potentiometer R7 Bourns Trimpot type 200L-1-101. 100 ohm

Transistor Q2 mounted on external heat sink on rear panel.

PLATE 18

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G82/3-118
6 VOLT REGULATED POWER SUPPLY PPI	

TO ACCOMPANY RECORD No 1968/32

RESISTORS.
Following resistors to be WELWYN "METOX" ½ WATT TYPE P20

R1 R2 R4	2.2K OHMS
R5	180 OHMS
R6	62 OHMS
R8	2.7K OHMS
R9	4.7K OHMS
R10	560 OHMS
R11	150 OHMS

POTENTIOMETER.
R7 BOURNS TRIMPOT TYPE 200L-1-101 100 OHMS
Available ex PAINTON Australia. Melbourne.

Following resistors to be WELWYN type AW3101 3 WATT W/W

R3	1 OHM
R3A	0.5 OHM

COMPONENT LIST.

CONNECTORS.

P1 P2	SOURIAU 8140-02 MALE 5 PIN
	VOCAB. SMZ198

TRANSISTORS.

Q1 Q4	TRANSISTOR TYPE T2309
Q2	TRANSISTOR TYPE OC36 or AN218
Q3 Q6	TRANSISTOR TYPE 2N404
	VOCAB. SVT/2N404
Q5	TRANSISTOR TYPE 2N861
	VOCAB. SVT/2N861

DIODES.

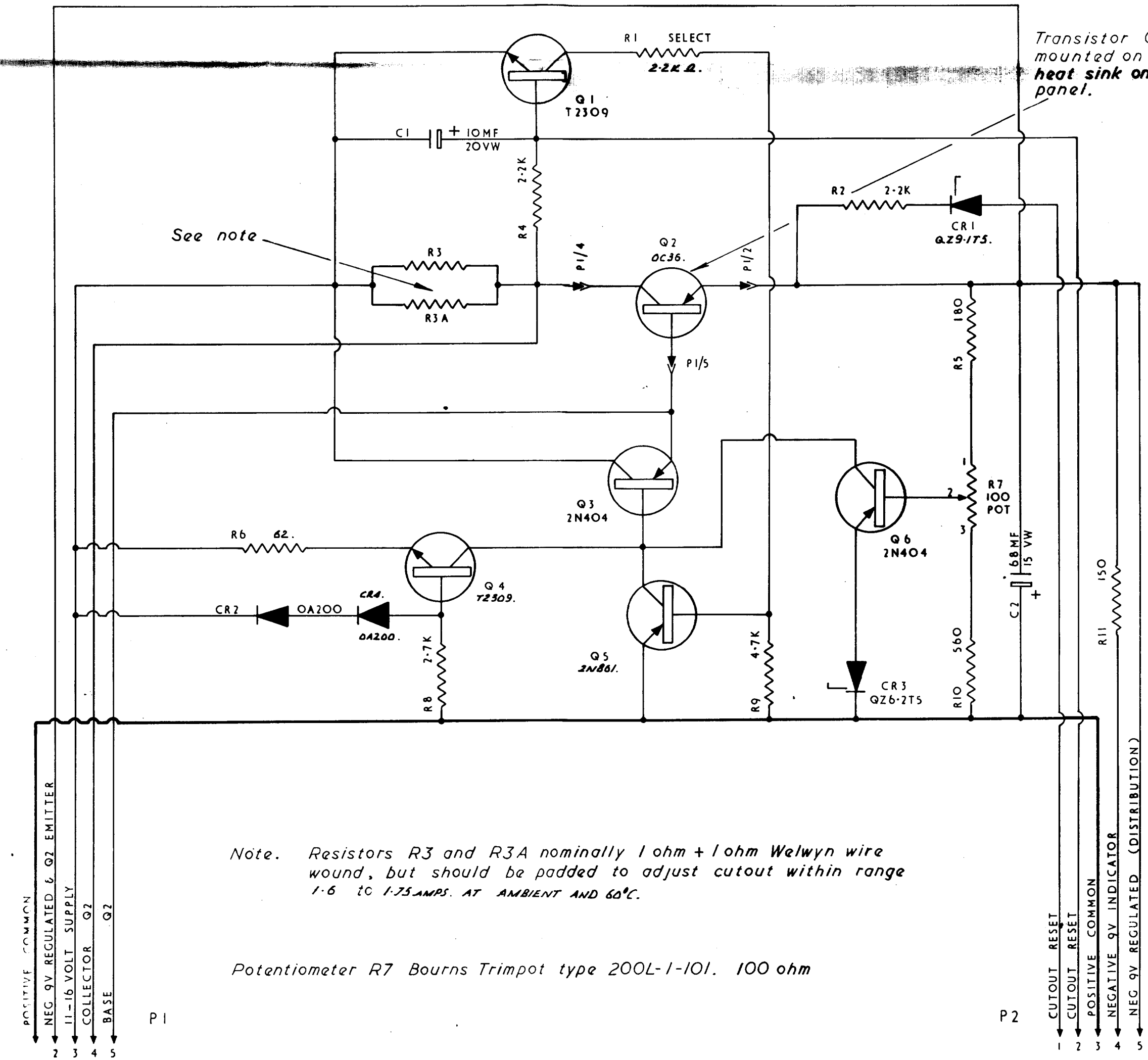
CR1	SILICON ZENER DIODE TYPE QZ9.1T5
	VOCAB. SVD/QZ9.1T5
CR2 CR4	SILICON DIODE TYPE OA200
	VOCAB. SVD/OA200
CR3	SILICON ZENER DIODE TYPE QZ6.2T5
	VOCAB. SVD/QZ6.2T5

CAPACITORS.

C1	TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D 106x0020 10MFD 20VW
C2	TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D 686x0015 68MFD 15VW

	DATE	NAME
Orig.	31 · 12 · 63	N D J
Amend.	12-5-64.	R. GAN.
	19 · 6 · 64	N D J

PLATE 19



Note. Resistors R3 and R3A nominally 1 ohm + 1 ohm Welwyn wire wound, but should be padded to adjust cutout within range 1·6 to 1·75 AMPS. AT AMBIENT AND 60°C.

Potentiometer R7 Bourns Trimpot type 200L-1-101. 100 ohm

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G 82/3 – 119	9 VOLT REGULATED POWER SUPPLY PP 2

TO ACCOMPANY RECORD No 1968/32

COMPONENT LIST.

CONNECTORS.

P1A P1B P2B	SOURIAU 8140-07 MALE 3 PIN
P2A	SOURIAU 8140-02 MALE 5 PIN VOCAB. BKZ198

TRANSISTORS.

Q1 Q2 Q3	TRANSISTOR TYPE T2309
Q4 Q7	TRANSISTOR TYPE 2N404 VOCAB. BVT/2N404
Q5	TRANSISTOR TYPE 2N301A VOCAB. BVT/2N301A Externally mounted.
Q6 Q6A	TRANSISTOR TYPE 2N277 VOCAB. BVT/2N277 Externally mounted.

DIODES.

CR1 CR7	SILICON ZENER DIODE TYPE 1Z8.2T5 VOCAB. BVD/1Z8.2T5
CR2 CR3 CR4 CR5	SILICON DIODE TYPE OA200 VOCAB. BVD/OA200
CR6	SILICON ZENER DIODE TYPE QZ6.2T5 VOCAB. BVD/QZ6.2T5

CAPACITORS.

C1	TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D 157x0015 150MFD 15VW
C2	TANTALUM ELECTROLYTIC SPRAGUE TYPE 150D 686x0015 68MFD 15VW

RESISTORS.

Following resistors to be WELWYN "METOX" ½ WATT TYPE F20

R1 R17	1K OHMS
R2 R16	330 OHMS
R4	12K OHMS
R5	270 OHMS
R6 R14 R15	47 OHMS
R8	2.7K OHMS
R9	5.6K OHMS
R10	620 OHMS
R11	150 OHMS
R12	10K OHMS
R13	1.6K OHMS

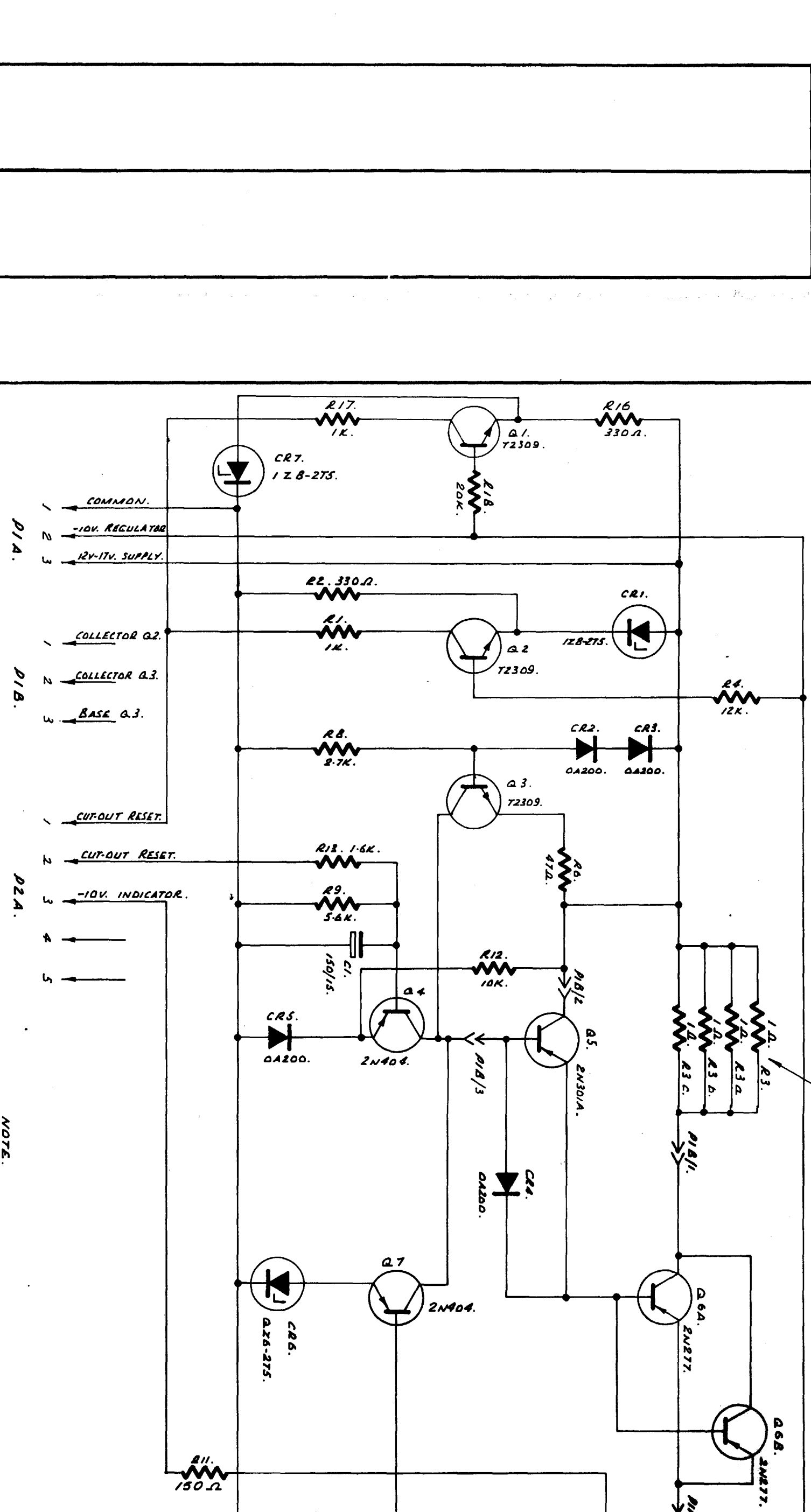
POTENTIOMETER.

R7	BOURNS TRIMPOT TYPE 200L-1-101 Available ex PAINTON Australia. Melbourne.	100 OHMS

Following resistors to be WELWYN type AW3101 3 WATT W/W

R3 R3A R3B R3C 1 OHM (Nominal)

	DATE	NAME
Orig.	12-5-64	R. GAN.
Amend.	29-5-64.	R. GAN.
	19 · 6 · 64	N D J
	27 · 7 · 64	N D J



NOTE.

REDRAWN WITH ADDITION OF CR3, CR7, Q1, R12-R18 TO ORIGINAL CIRCUIT.

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G82/3-120	10 VOLT REGULATED POWER SUPPLY PP3

TO ACCOMPANY RECORD No 1968/32

PLATE 20

COMPONENT LIST.

CONNECTORS.

P1 P2	SOURIAU 8140-02 MALE 5 PIN VOCAB. BKZ198

TRANSISTORS.

Q1 Q2	TRANSISTOR TYPE 2N427
Q3	TRANSISTOR TYPE 2N398A

DIODES.

CR1 CR2 CR3 CR4	SILICON DIODE TYPE OA202 VOCAB. BVD/OA202
CR5	SILICON DIODE TYPE OA200 VOCAB. BVD/OA200
CR6	SILICON ZENER DIODE TYPE QZ4.7T5 VOCAB. BVD/QZ4.7T5

CAPACITORS.

C1 C2	DUCON STYROSEAL TYPE DFB610 600VW 680 PF VOCAB. BCP6681
C3	PHILIPS POLYESTER TYPE C296 125VW 1 MFD VOCAB. BC01105

RESISTORS.

Following resistors to be WELWYN "METOX" ½ WATT TYPE F20

R1 R2	360 OHMS
R3	10K OHMS
R4 R5 R6	82K OHMS
R7	47K OHMS
R8	2K OHMS

R9 VOLTAGE DEPENDENT RESISTOR PHILIPS TYPE E299DG/P224

TRANSFORMER T1.

PHILIPS POT CORE TYPE D25/16

Air gap 0.25 mm.

½ primary turns. 128 turns No.32 B & S double solderite wire.

½ feedback turns. 64 turns No.39 B & S double solderite wire.

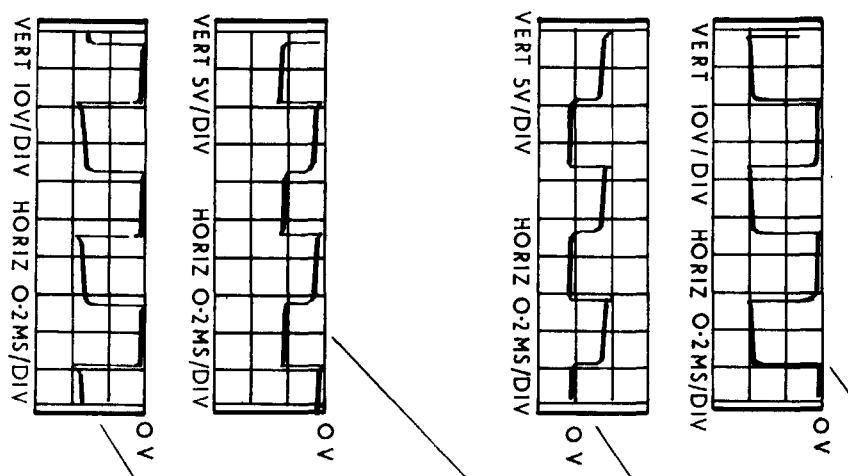
Secondary. 1600 turns No.40 B & S double solderite wire.

Fit 2 turns of .001" paper between feedback and primary.
Fit 2 turns of .002" paper between primary and secondary.

Former to be wax impregnated. Use "OKERIN" type 561.

Reference S16.

	NAME	DATE
Orig.	N D J	9 · 8 · 63
Amend.	N D J	20 · 12 · 63
	N D J	19 · 6 · 64



BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS

Drawing No. G82/3-121

90VOLT REGULATED POWER SUPPLY PP4

TO ACCOMPANY RECORD No 1968/32

PLATE 21

REAR.

AM3. AM1.

J2/1 J2 2A 2B J2/3 J2/4

PP3. AM2.

J4 1A 1B J4 2A 2B J4/3 J4/4

PIN NUMBERING ALL CONNECTORS.

J3/2 J3/3 J3/4

TDI.

SA2. SA3.

J13/1 J13/2 J13/3 J13 4A 4B

PP4. DV3.

J12/1 J12/2 J12/3 J12/4

SA4. DV3.

J11/1 J11/2 J11/3 J11/4

DV2. SA1.

J10/1 J10/2 J10/3 J10/4

DV2. DV1.

J9/1 J9/2 J9/3 J9/4

PP2. DV1.

J8/1 J8/2 J8/3 J8/4

O1.

J7/3 J7/4

CRYSTAL OVEN.

PP1.

J6/3 J6/4

FEED THRU CAPACITORS.

FRONT.

PLAN VIEW

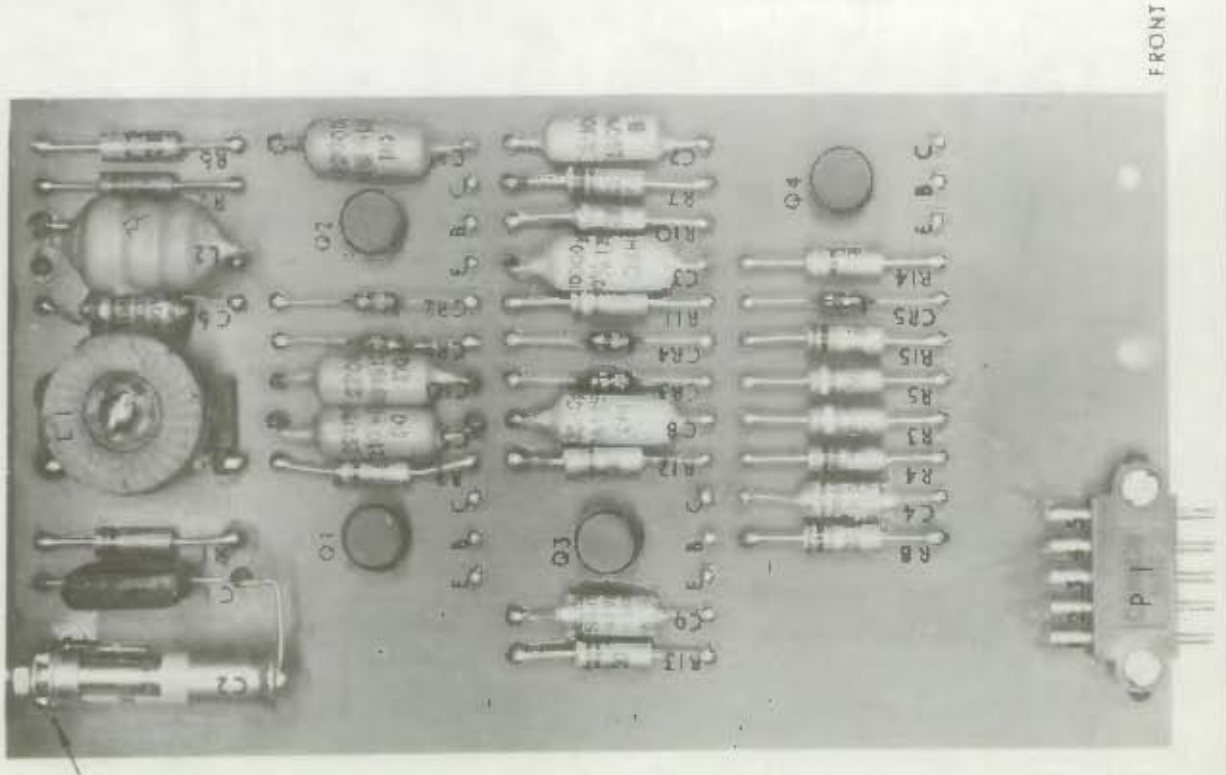
BUREAU OF MINERAL RESOURCES GEOLOGY AND GEOPHYSICS 485 BOURKE STREET, MELBOURNE, VICTORIA GEOPHYSICAL LABORATORIES, FOOTSCRAY	MATERIAL	DATE 10-7-64.	PLAN OF CARD POSITIONS	DRAWING No. G82/3-122
	SCALE.	NAME R. G. AN.		

TO .ACCOMPANY RECORD No 1968/32

DATE	DRAWN	AMENDMENTS.	ISSUE
29-5-64.	R.GAN.		1.
25·6·64	N.D.J		1.
6-10-65	R.G.	VARIOUS.	2.

RECORD No 1968/32

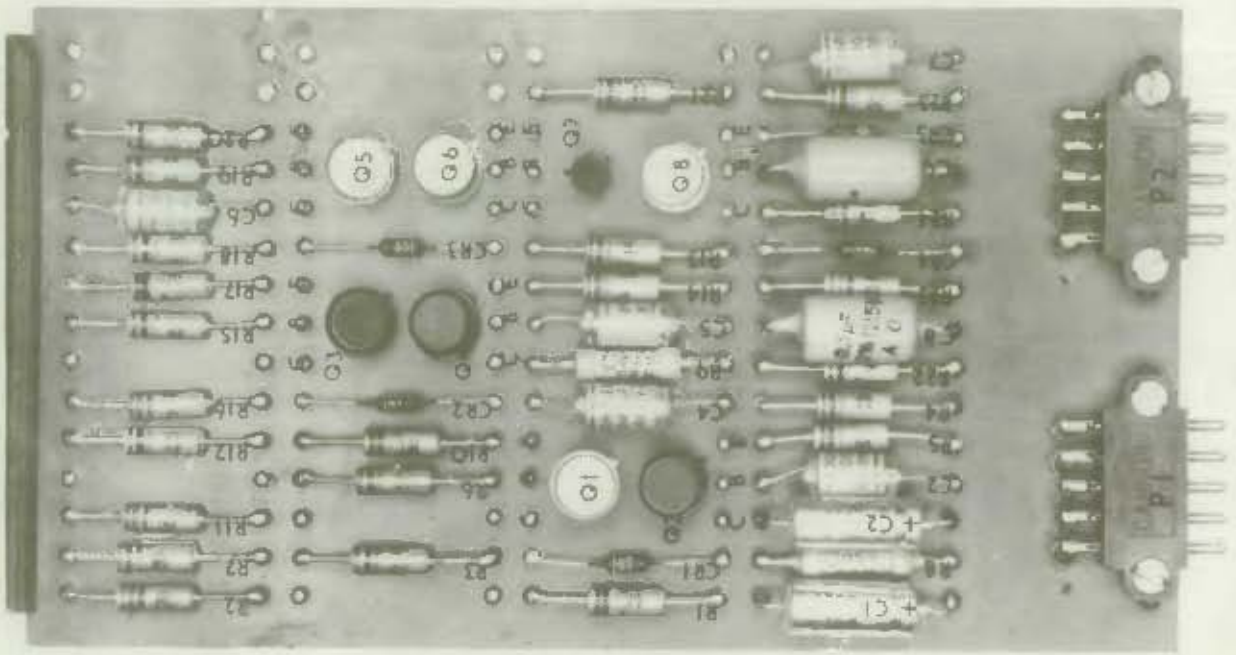
BUREAU OF MINERAL RESOURCES GEOLOGY & GEOPHYSICS.	DRAWING No. G82/3—123	MAIN CHASSIS WIRING, SCHEMATIC DIAGRAM



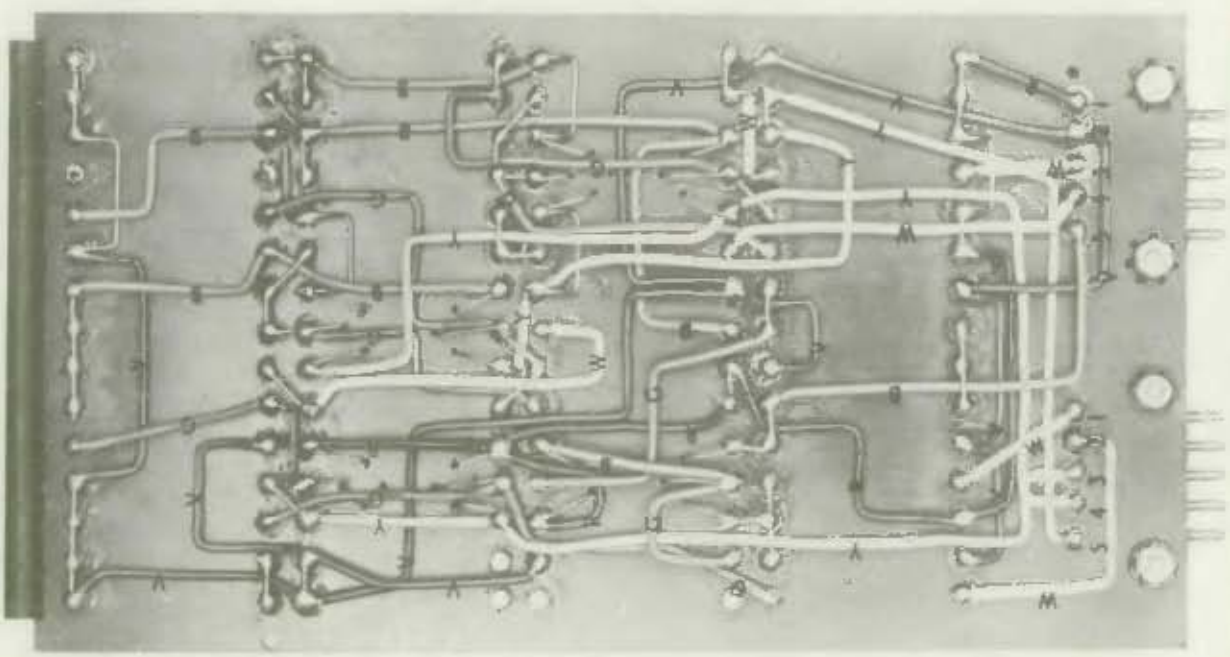
OSCILLATOR UNIT 01
COMPONENT AND WIRING LAYOUT

To Accompany Record Number 1958/32

FRONT



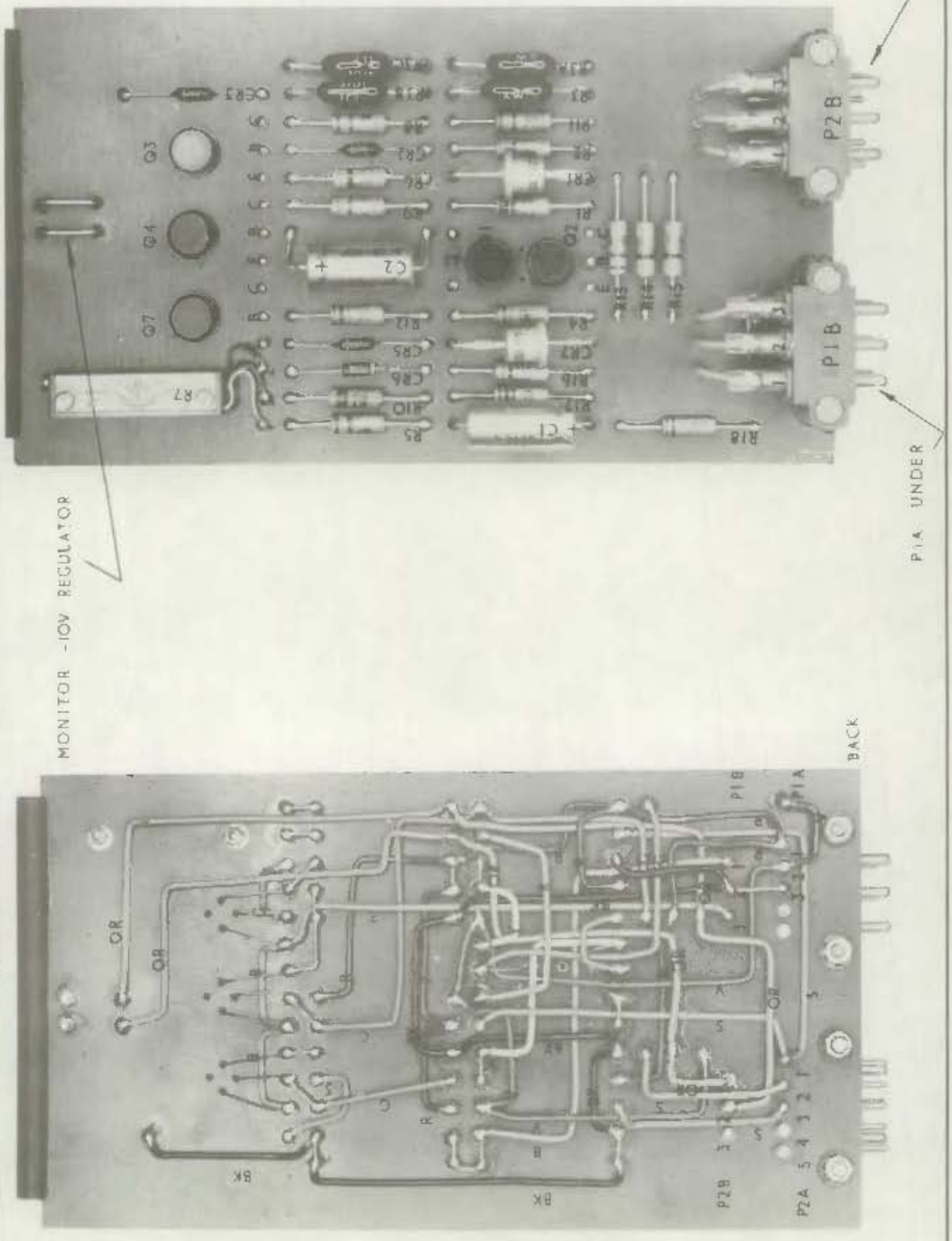
BACK



TIME COMPARATOR UNIT SA4
COMPONENT AND WIRING LAYOUT

To Accompany Record Number 1968/32

PLATE 26



-10 VOLT REGULATED POWER SUPPLY UNIT PP3

COMPONENTS AND WIRING LAYOUT

To Accompany Record Number 1968/32

G82/3-126

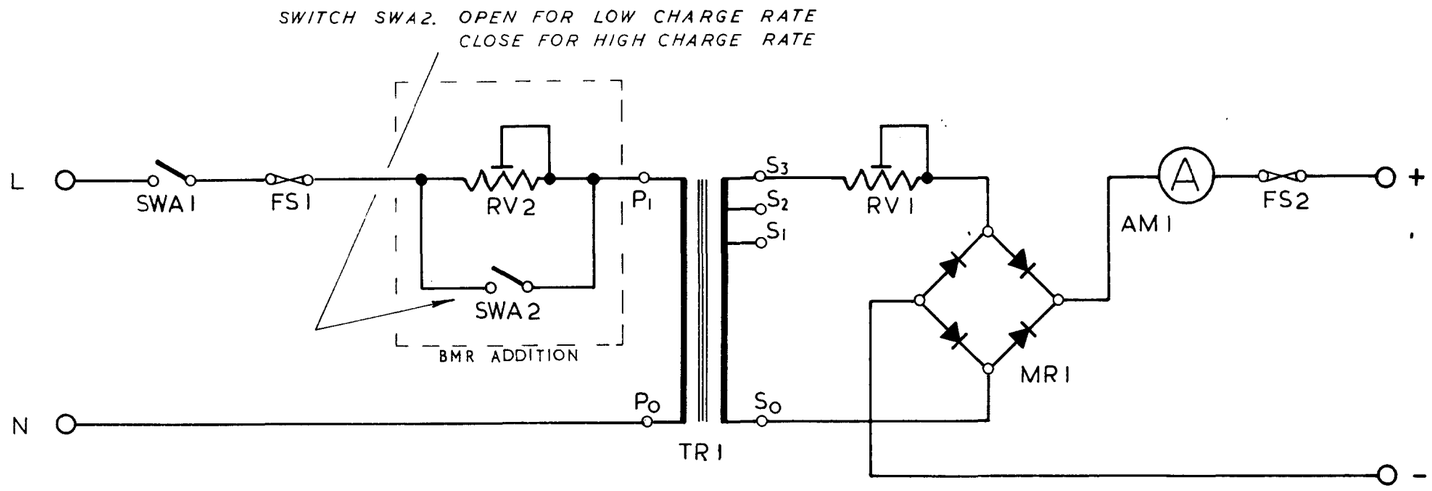
	DATE	NAME
Orig.	7 · 7 · 64	N D J
Amend.	13 · 8 · 64	N D J

REFERENCE Mc KENZIE AND HOLLAND (AUSTRALIA.) PTY. LTD.

~~SPECIFICATION Nº MR 476/541~~

SHEET 5 OF 5 SHEETS.

17-2-64.



Note. Select tap S1, S2 or S3 for required output current in conjunction with Ballast Resistor RV1.

SWITCH SWA2. CUTLER HAMMER TOGGLE 250V 3A SP. ST. VOCAB. BST II
RESISTOR RV2. DUCON ADJUSTABLE TYPE HO WITH V TYPE COATING. RES 100 OHM. TERMINALS TYPE 4

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS	Drawing No. G82/3-127	BATTERY CHARGER