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NOTES ON INTERFACING ELECTRONIC EQUIPMENT WITH SPECIAL REFERENCE TO THE 1977 MARINE DATA ACQUISITION SYSTEM

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CONTENTS

SUMMARY

One of the more subtle problems in designing electronic hardware systems is that of interconnecting the component instruments without degrading system performance. Such successful interfacing is more difficult when low-level or high-speed signals are present, especially in mobile systems subjected to vibration, electromagnetic interference, and ground current loops. The mechanisms of these and other detrimental effects are discussed, and general recommendations given for both analogue and digital signal interfacing.

The data acquisition system for the marine survey, originally programmed for 1977, must be designed before the system components are to hand, and without knowledge of the survey vessel. Specific recommendations made for the marine system should ensure a high level of interfacing flexibility and minimize interference from other systems in the ship.

Notes on Interfacing Electronic Equipment with Special References to the 1977 Marine Data Acquisition System

K.J. Seers

1. Introduction

This set of notes arose from the involvement of the electronic laboratories in the design of the data acquisition system for the 1977 marine survey.

To ensure maximum system flexibility and ease of implementation, various interfacing circuits and practices were recommended which could add as much as $33 000 to the cost of the system. These notes provide the technical background on which the recommendations were based and were written mainly to justify the additional expenditure, and to indicate the philosophy of the design.

The problems considered in subsequent sections are not unique to the marine system, being especially pertinent to vehicle-borne systems and systems whose components are separated by moderate distances. The material is therefore presented in tutorial form as it may have applications in other areas and could be useful to technical staff. The selection of material is derived from past experience with marine, airborne, and other systems, supplemented by information culled from books and papers in the bibliography.

Electronic technology has a very short "half-life". The development of current injection logic and signal transmission via fibre-optics will probably effect a major change in interfacing techniques within two or three years. These notes, however, are concerned only with the present "state of the art".

2. The Interfacing Problem

When connecting two or more instruments together two tacit assumptions are usually made:

1. Signal information is not modified by the connection.

2. Information fed into the connecting medium at one end is identical with that delivered by it at the other end.

In general these assumptions are not valid; the problem in interfacing is to determine the conditions required to make them valid in a given situation.

The first assumption is basically concerned with loading effects and can be satisfied by careful matching of source to load, remembering that the distributed inductance, capacitance, and resistance of the connecting cable form part of the load.

The second assumption refers to noise originating either from external sources, or by virtue of the connection itself. In this context noise means anything added to (or deleted from) the desired information and therefore includes signal distortion.

3. Noise - Causes and Treatment

This topic has been extensively treated in the literature, so this section is limited to a very brief review. There is, however, some detailed discussion of subjects, such as ground noise, which are particularly relevant.

Only system noise is considered, the design of low-noise instruments being outside the scope of these notes.

3.1 Electrostatic Coupling

If a signal line passes close to a source of varying potential, the capacitance between the line and the source will couple the variations to the signal line, thus introducing noise.

Capacitively coupled noise can be eliminated by interposing a conductive shield held at constant potential with respect to the signal - usually at signal ground. The requirement for constant potential implies that no currents from external circuits flow in the shield; it should therefore be grounded at only one point.

3.2 Magnetic Coupling

Magnetic field changes, produced by current changes in one conductor, will induce voltages in adjacent conductors.

To minimise such induced noise, all circuits, whether power or signal, should use pairs of conductors, with the return line of the pair kept close to (preferably twisted with) the main line; both interfering fields and induced voltages then tend to cancel.

Magnetic shielding is difficult and costly, requiring special alloys such as mu-metal, conetic, and netic. Often, several layers of various materials are needed to combine high permeability and high saturation flux density.

Physical separation of interacting circuits, if possible, is preferable to magnetic shielding. If circuits are run in pairs, the intensity of the interference reduces with distance at a rate approaching an inverse cube law. Signal and power circuits should always be separated.

3.3 Electromagnetic Coupling

When the signal wavelength is short compared with the transmission distance, it is not valid to regard the signal as current flowing in the conductors; rather, an electromagnetic field is propagated in the space between the conductors. If there are discontinuities in conductor geometry, energy can be lost as radiation. Similarly, radiated energy can be absorbed at discontinuities. For the dimensions of the systems being considered, electromagnetic coupling can occur only at radio frequencies.

Rf interference can be avoided by treating all interconnections longer than a quarter wavelength as transmission lines. This implies a constant characteristic impedance along the entire interconnecting path.

Shielding is also effective at radio frequencies; but it is unfortunate that the single ground point, required for electrostatic shielding, is unsuitable for rf, where multiple-point bonding to ground is necessary. This difficulty can be overcome by the use of double shields, or a single shield grounded at one point and rf-bypassed at others.

In general, the elimination of rf interference poses problems which are unique to each system, and a thorough understanding of the various interference mechanisms is essential.

3.4 Microphony

Microphony is a general term covering any electrical noise produced by mechanical stimulus. Mobile systems are more prone to microphony than static systems, and the usual solutions involve shock-mounting of instruments and/or equipment racks.

A type of microphony often overlooked is cable noise. Cable movement produces friction between conductor insulators, thus developing static charges. The generation and subsequent redistribution of these charges causes noise to be capacitively coupled into the signal conductors.

It is therefore desirable to transmit signals along cables at high levels (volts rather than millivolts), and to amplify low level signals as close as possible to the source, keeping low level cables as short as possible. All cables should be securely tied down, unstressed, and protected from foot traffic etc.

3.5 Ground Noise

Ground noise is probably the most insidious and ubiquitous noise source in systems implementation. It arises from the grounding of various electrical and electronic systems (power,

lighting, control, communications, alarm, navigation, battery-charging, etc.) to the frame of the ship, aircraft, etc. Even when a two-wire power and signal system is used, equipment is not usually insulated from frame, and return currents tend to flow through it.

The vehicle frame may therefore be represented by a very complex multi-mesh equivalent circuit containing a multitude of voltage generators having various frequency and transient characteristics.

The sub-systems installed for survey operation (e.g. navigation, gravity, magnetic, data acquisition) will, in general, be located at various parts of the vehicle and grounded at those locations. If the sub-systems are connected together directly, the data acquisition instruments will measure input signals with reference to one ground point while the outputs from the other sub-systems will each be referred to a different ground point. As these ground points may be at different and varying potentials, the signals seen by the data acquisition system may be in error.

Typical magnitudes of error voltages range from millivolts to volts, and there is little to be gained by simply joining the ground points with a cable; this merely adds another mesh to an already low-resistance equivalent circuit. Some method of reducing the errors must be used, however, as the magnitudes can be large enough to invalidate most data inputs, whether digital or analogue.

The simplest methods for digital systems are: the use of differential drivers and receivers, or optical isolation. If properly implemented, optical isolation is superior electrically and requires less power.

Analogue systems should have differential inputs with high common mode rejection. This allows signals to be measured with respect to the source ground, regardless of ground differences.

3.6 Electro-Chemical Ground Noise

Dissimilar metals in contact generate an electric potential and, in the presence of moisture, currents may flow if the circuit is completed in an unbalanced manner. (The action of the electrolyte so formed produces bimetallic corrosion). The marine environment is highly conducive to this process, which adds further noise sources to the equivalent circuit previously mentioned.

3.7 Rack Ground Noise

Most instruments are packaged in metal bins or cabinets which, if connected to a suitable potential, act as electrostatic shields. Normally, the bin should be at instrument ground potential. Instruments, which together form a sub-system, are usually bolted into a metal rack which assumes sub-system ground potential via the bolts and bins. The rack, is usually bolted to the vehicle frame at more than one point, allowing ground currents to flow through the rack and bins, thus setting up varying ground references for each instrument.

In one of the Bureau's airborne installations, significant ground noise may be observed, on an oscilloscope, between racks less than one metre apart.

Ideally, racks should be installed on insulating mounts, and bonded to ground at one common point for each subsystem. The bonding braid should be as thick (and as short) as possible, because its self-inductance significantly increases its impedance with frequency.

A similar noise source originates from current flow between bins in the same rack. This is more common on dc powered equipment, in which the power ground connects to the bin, and the resistance of the dc return lead is greater than that of the alternative return path through the rack and frame. With most commercial instruments very little can be done about this, except to use ground return leads of the heaviest convenient gauge, and in stubborn cases to insulate the bin from the rack.

It is often worthwhile to construct instruments without a permanent internal connection between power ground and bin, but, by means of a grounding link on the rear panel, to provide the option of grounding the bin to the power ground or, when bolted to the rack, to the rack only. The latter configuration is only fully effective when currents cannot flow in the rack, the bin then being at a constant potential and unable to couple noise electrostatically to internal circuits.

3.8 Self-Generated Ground Noise

This occurs most frequently in digital systems using fast switching logic families, such as transistor-transistor logic (TTL). As previously stated, interconnections longer than one quarter wavelength of the highest-frequency component in the switching waveform should be treated as transmission lines. Usually, one side of the line is a ground connection; failure to carry this right through from device to device not only produces pulse reflections due to abrupt impedance change, but diverts energy to the power-supply ground networks associated with the

source and load devices. At low frequencies these networks have almost zero impedance, but distributed inductance and capacitance turn them into highly resonant circuits at high frequencies (typically a few megahertz). When these networks are subjected to a fast pulse, ringing will occur at the natural resonant frequences, and will be impressed on the ground reference points for other devices in the instrument. As the ringing can be up to several volts in amplitude, false triggering can occur. Even much lower amplitudes will seriously degrade the logic noise immunity - only 0.4 volts worse case for TTL.

3.9 Self-Generated Signal Noise

This takes two main forms: The first is waveform distortion caused by the inability of a signal source to drive its load. The solution is simple; if neither source nor load can be suitably modified, some form of buffer circuit should be interposed.

The second form occurs when transmission lines are incorrectly terminated. Pulse reflections can cause false operation and possibly damage devices. This is treated more fully in Section 4.

3.10 Power-Supply Noise

Noise, inevitably present on power-supply lines, can be coupled into signal circuits. Sound instrument design will preclude this, but occasionally, special external circuits are necessary (filters, regulators, double-shielded transformers, etc.).

4. Problems with High-Speed Logic

If high-speed logic causes problems, why use it? There are two reasons: Firstly, although various logic families are used within instruments, TTL is by far the most common family used to interface between instruments, because of advantages deriving from cost, speed, and ability to drive low load resistances and long lines. Because TTL is virtually an industry standard, and we obtain data mainly from commercial instruments, we are forced to use it.

Secondly, in a computer-based data acquisition system, data is sampled by the computer in multi-bit words, and all bits comprising a word must have settled to their correct logic level when sampled. With typical sampling times less than a microsecond and asynchronous operation, slowly settling logic could produce a high error rate.

Most problems associated with interfacing TTL systems stem from the high-frequency content in a TTL switching transition. With typical rise and fall times of 10 nanoseconds or less, frequencies from dc to well above 100 megahertz are present. Minimum wavelengths are about one metre, so that all interconnections longer than 0.25 metre must be regarded as transmission lines.

4.1 Line Driving Problems

As indicated previously, discontinuities in the transmission line will produce reflections and energy loss by radiation. The results are waveform degradation, cross-talk, and self-generated ground noise.

The number and amplitudes of pulse reflections depend on the degree of mis-match between source, line, and load. Input and output impedances of TTL gates are very different, extremely non-linear, and change with logic state, thus precluding the use of linear analysis. However, the reflections can be predicted quite accurately via the Bergeron diagram - a graphical technique which assumes a constant-impedance transmission line, and a knowledge of input and output characteristics of the source and load devices. Figure 1 illustrates waveforms possible without any type of line termination.

4.1.1. Long Settling Times

In Figure 1, both sending and receiving waveforms approach their final values in a number of steps, each of which lasts for twice the propagation delay of the line (Tp approx. 5 nanoseconds per metre). Thus, in the absence of any form of line termination, a logic step could take well over a microsecond to settle.

4.1.2. Uncertain Switching Levels

The amplitude of step B1 in the sending waveform increases with increasing line impedance and decreases with increasing values of internal pull-up resistance in the TTL output stage. B1 frequently occurs at an amplitude of about half logic swing and is therefore very close to the switching threshold. If any other gate input were connected to this point, its noise immunity would be essentially zero. It is therefore sound practice to ensure that a gate used to drive a line is not used for any other purpose, and that flip-flops are never used to drive lines - the regenerative action required relies on a rapid output transition internally coupled back to the input.

Level B2 reduces with increasing line impedance and increases with increasing saturation resistance of the TTL output stage. Both B1 and B2 increase with increasing reverse current

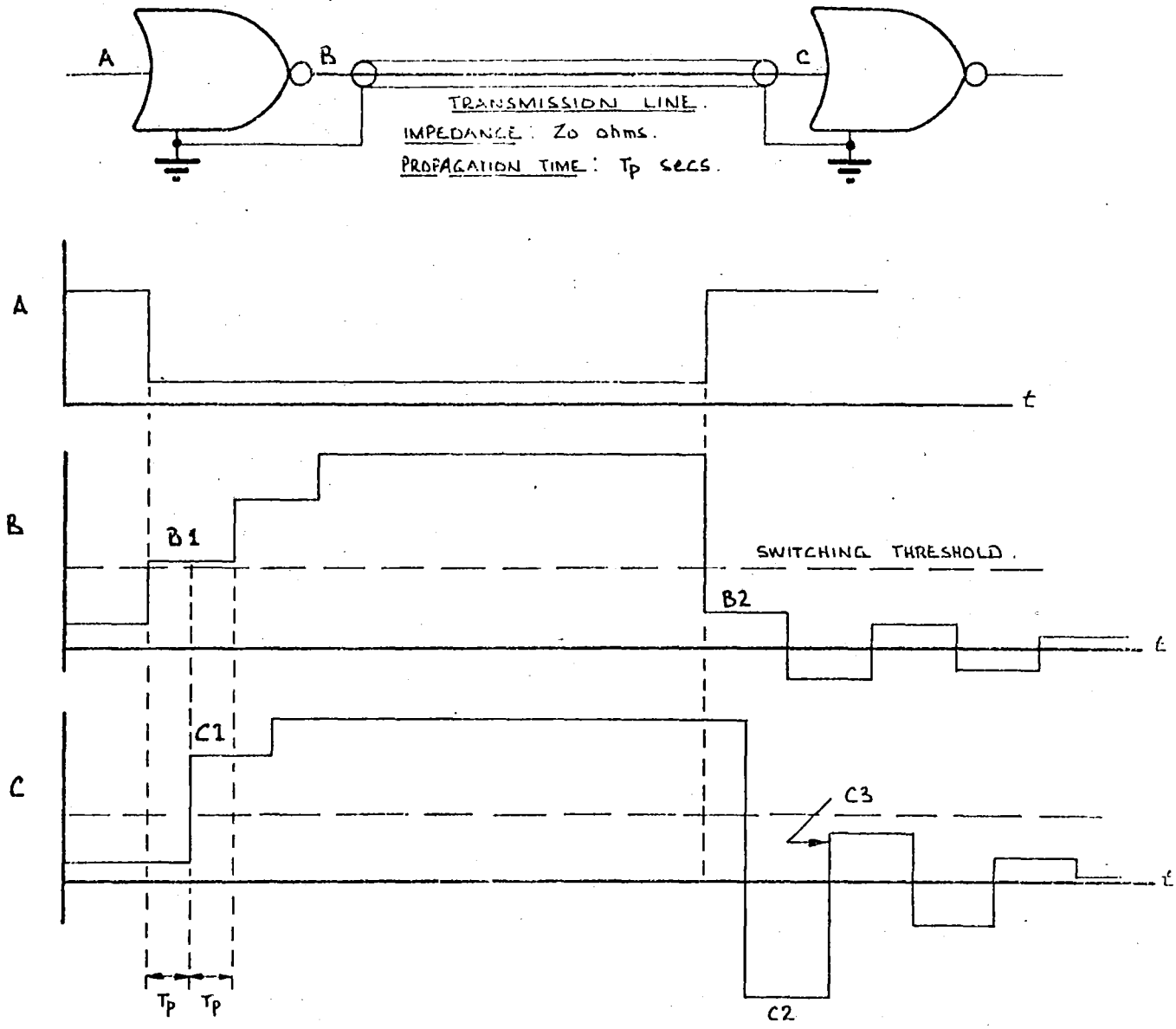


Figure 1. TTL Waveforms with Unterminated Line.

gain in the TTL output pull-down transistor. B1, however, is usually the closer to the switching threshold. At level B2 the driving output stage is required to sink currents which may be well in excess of 50 milliamps. With high pulse frequencies and long lines, care must be taken to ensure that the device is not subjected to excessive power dissipation.

At the receiving end of the line, level C1 is always greater than B1 by an amount which increases with increasing line impedance. In some situations, C1 can be very close to switching threshold, and, if the propagation time is long enough, noise can produce multiple pulses at the output of the receiving gate. If line impedance is high, C1 can be above the final steady-stage level: overshoot can occur. In fact if line impedance exceeds about 300 ohms, C1 will exceed 5.5 volts (the maximum allowable input voltage) and the receiving gate may be damaged.

The undershoot at C2 is clamped to about one volt in most TTL devices by internal diodes designed for this purpose. Without these diodes the undershoot would be proportional to line impedance and might reach -3.5 volts even with a line impedance of 100 ohms. There is variation among device types, and between manufacturers, in the degree of clamping provided. Some devices have no diodes at all and would be damaged by this reverse pulse. Diode clamp characteristics should always be considered when selecting a line receiver.

A poor clamp diode, combined with high line impedance, can cause the level at C3 to exceed the switching threshold, thus re-triggering the receiving gate. Even when the effect is less drastic, the noise immunity of the receiving gate is reduced for the duration of level C3.

Because levels B1, B2, C1, C2, and C3 all depend on integrated circuit characteristics (as well as line impedance), there will be a large spread between manufacturers, between devices from the same manufacturer, and, most of all, with temperature changes in a given device. Some form of impedance matching is desirable to reduce reflections and thereby reduce the steps and their variations in both the send and receive waveforms.

Discontinuities in the transmission line will exacerbate all of the hazards mentioned above, as well as producing cross-talk and ground noise.

4.2 Matching TTL Transmission Lines

A transmission line terminated by a resistance equal to the characteristic impedance of the line will not produce reflections from the receiving end. This would require the

receiving gate to be shunted with a resistance of between 50 and 200 ohms, depending on the type of line. Unfortunately, ordinary gates used as drivers cannot supply sufficient current to maintain proper logic levels across such low resistances. Even special gates designed to drive a 50-ohm terminated line can guarantee a high level of only 2 volts worst case, thus reducing the noise immunity to zero. Also, high power is required to drive shunt-terminated lines, although this can be reduced by ac coupling of the termination.

An alternative technique, known as series or reverse termination, uses a resistor in series with the sending end of the line, leaving the receiving end connected to the receiving gate only. The resistor value is such as to make the effective output resistance of the driver approximate the line impedance in both the low and high logic states. Reflections from the receiving end are almost completely absorbed at the sending end.

An improved reverse termination method, due to B.C. Gilbert of the ATC Research Laboratories, provides virtually exact matching of source to line in both high and low states. The method is very effective and is recommended as standard BMR practice. Figure 2 illustrates the method.

The only distortion in the received waveform is an unavoidable time shift due to the propogation time of the line.

Resistors R 1 and R2 are given by

$$R1 = Zo - Rp$$
$$R2 = Rp$$

where Rp is the effective internal pull-up resistance in the TTL output stage. (The saturation resistance of the pull-down transistor is assumed negligible).

Diode CR1 shorts out R2 in the high logic state, giving an effective driving resistance of Zo in both logic states. CR1 must be a fast switching diode with low forward voltage drop; a Schottky barrier diode is recommended.

Levels B1 and B2 still occur at the sending end, so it is still bad practice to connect any other gate input to this point. B2, however, is higher than before, being very close to B1, and demanding less current than previously.

The receiving waveform is free of steps, undershoot, and overshoot. There are thus no problems of device degradation or multiple triggering, no dependence on clamp diodes, and the noise immunity is restored almost to normal.

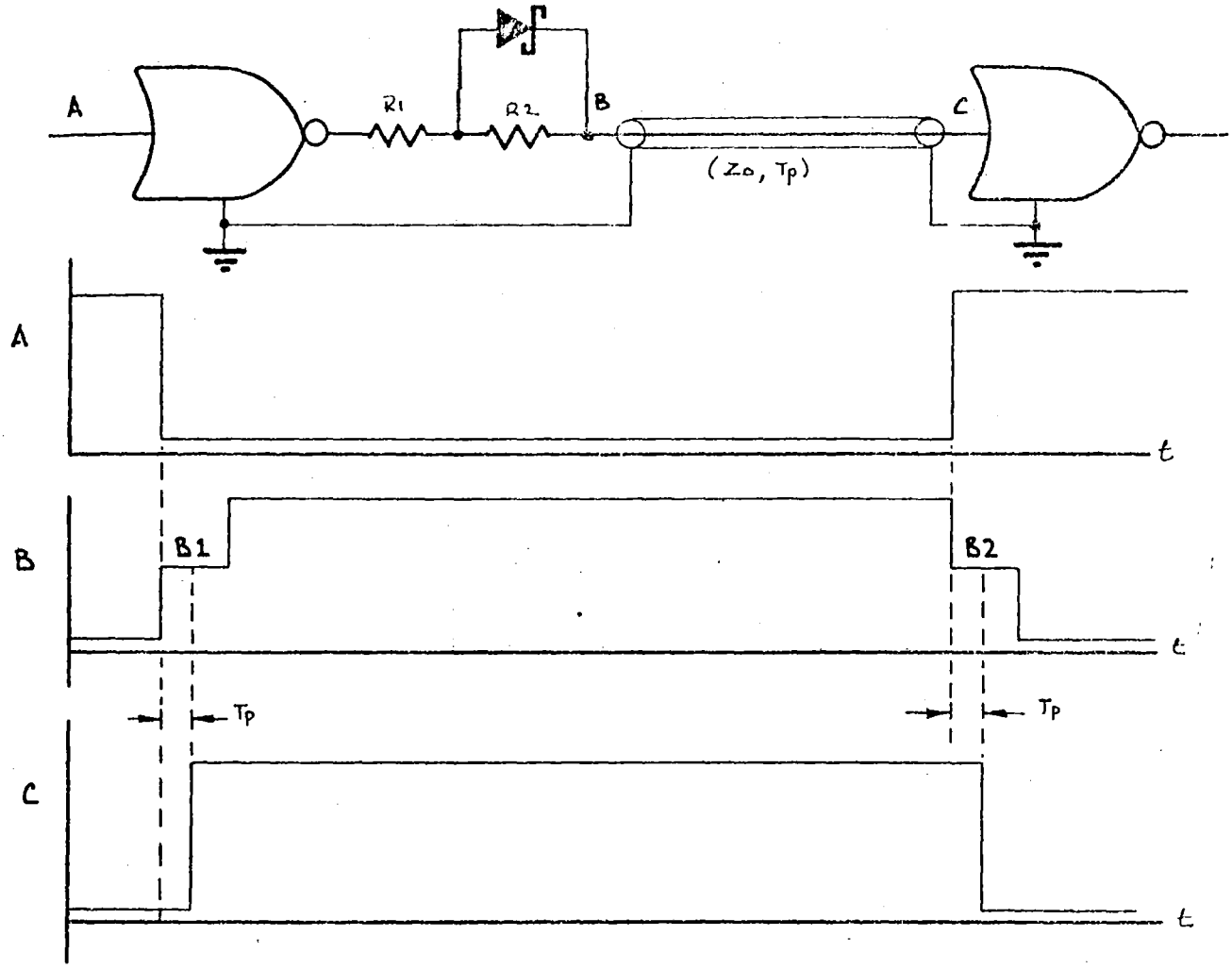


Figure 2. TTL Waveforms with Gilbert's Reverse Termination.

4.3 Selecting a Cable for Logic Transmission

Only two cable types are normally considered:

Co-axial cable is the better, if performance is the only criterion, because of its uniform properties. It can be obtained with characteristic impedance ranging from 25 ohms to 125 ohms, the higher values being more suited to reverse termination techniques. The disadvantages are cost, bulk, and the special multi-pole connectors required for multiple lines.

Twisted pair does not perform so well as co-axial cable because of less uniform coupling between the two sides of the line; there is consequently more chance of cross-talk between adjacent lines. Depending on geometry, impedances range from

about 70 ohms to 200 ohms, better performance being obtained from the low values. The advantages are low cost, small size, and the ease of using ordinary connectors (at the expense of uniform impedance).

5. General Recommendations for Analogue Interfacing

Referring to Section 3, the main sources of interference in analogue systems are electrostatically coupled noise, magnetically coupled noise, and ground noise. Electromagnetic noise is not considered because the analogue systems of interest operate at low frequencies.

In addition to the recommendations already made in Section 3 regarding rack earthing, etc., the following recommendations should be followed to reduce interference from the above sources:

1. Connect to the signal source differentially, even if one line is at source ground.

2. Use differential input circuits having high common mode rejection.

3. Amplify low-level signals as close to their source as possible and distribute them at moderate voltages (say $\pm$ 10 volts full scale).

4. Use one twisted shielded pair for each signal channel, grounding the shield at only one point, preferably at the source end. If the source is floating, it may be better to ground the shield at the amplifier input stage. Ensure that shields from different cables do not touch at any point other than their designated ground points. Never use ordinary co-axial cable; for low-level signals use a low-noise cable such as Belden 8428. Ensure that all cables are securely fastened, unstressed, and protected.

6. General Recommendations for Digital Interfacing

TTL logic is assumed.

The main interference sources are ground noise, self-generated signal noise, self-generated ground noise, and rf interference most frequently occurring as cross-talk. The last three sources of interference are all likely to arise from poor line-driving techniques. The following recommendations apply:

1. Use opto-isolators to reduce ground noise. (An opto-isolator consists of a light source driven from the sending circuit, and optically coupled to a photo-transistor connected to and receiving its ground reference from the receiving circuit.) A suitable type is HP5082-4364, a dual TTL-compatible isolator in an 8-pin package.

2. For line driving, use Gilbert's reverse termination and a driving device, capable of driving capacitive loads, such as the SN74128N quad 2-input positive-nor 50-ohm line driver. The following circuit (Fig. 3) is recommended for 80-ohm twisted-pair cable: (for other impedances change R1 - see Section 4.2).

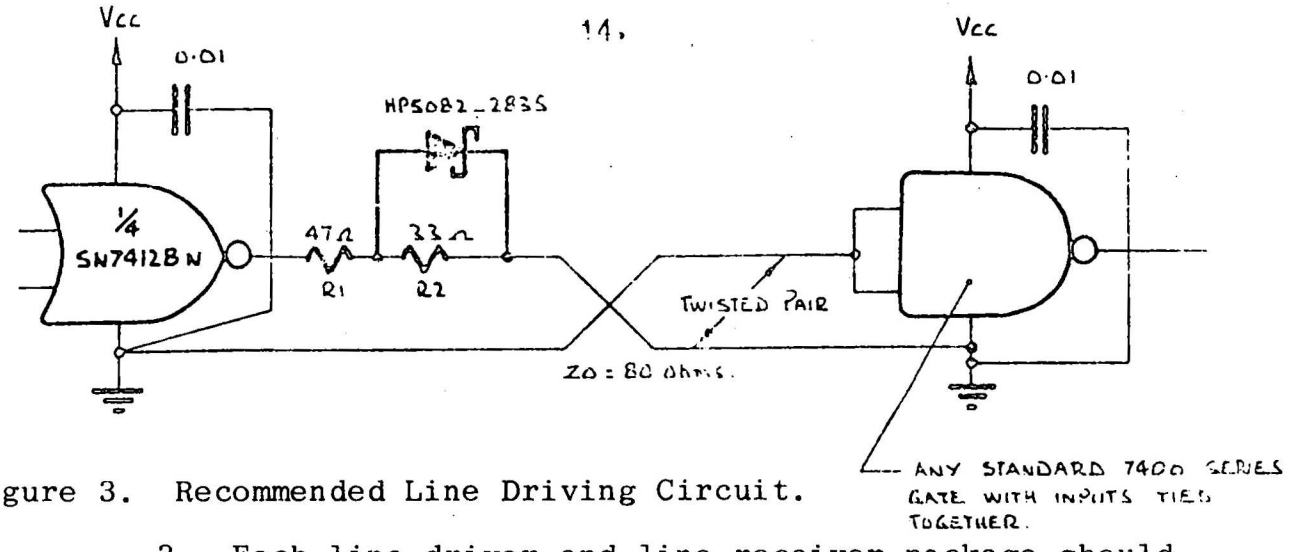


Figure 3. Recommended Line Driving Circuit.

3. Each line driver and line receiver package should be individually bypassed with a high-quality rf capacitor located as near as possible to the package and having minimum lead length. This ensures that the high currents required during switching are available at the points of demand and do not produce power-supply noise at other devices. 10 000 pF capacitors, such as Vitramon VK44BA103, are suitable.

4. Line driving and receiving gates should not be used for any other purpose. Multiple inputs on receiver gates should be tied together. Avoid connecting other gates to driver outputs.

5. For short lines (up to a few metres) standard gates with Gilbert's reverse termination may be used as drivers, but on no account should flip-flops or other commutating circuits be used.

6. Twisted-pair transmission line should be used for all interconnections longer than 0.25 metre. (Coaxial cable is preferable if cost and bulk are unimportant). Wherever possible, the transmission line should be continued through instrument connectors, back-plane wiring, circuit board connectors, and right up to the sending and receiving devices. A single-point ground is desirable for the package, transmission line return, and bypass capacitor.

7. If it is impracticable to continue the line right to the device on a printed circuit board, then a printed microstrip transmission line having the same impedance may be used at the expense of increased cross-talk. A microstrip line consists of a conductor on one side of the board and a ground plane on the other side. For 1/16 inch fibreglass board with 2-ounce copper on each side, the conductor width for a given impedance Zo ohms is given approximately by

$$W \quad 0.447 \exp \quad -Zo(0.0295) \quad - 0.0034 \text{ inches}$$

which gives a value of 0.039 inches for an 80-ohm line. Care should be taken to eliminate power-supply ground currents, associated with other circuits, from flowing in the ground plane. Note that a ground plane is always desirable, whether part of a microstrip line or otherwise.

8. To assist in restoring line balance degraded by connectors, circuit board wiring, etc., each twisted pair running between the instrument connector and circuit board back-plane should be wound several times through a small, high-permeability, ferrite toroid or screening bead. This has a differential inductive effect, resisting current differences between the two sides of the line. Both sending and receiving instruments should be treated in this way. A suitable toroid is Philips 4322-020-9100.

9. Direct single-wire connections without a ground plane should never exceed 0.1 metre; they may be extended to 0.25 metre with a ground plane.

7. Specific Recommendations for 1977 Marine System

7.1 System Configuration

At the time of writing, the fine detail of the system has not been fully specified, but a preliminary detailed block diagram has been prepared and is appended to these notes.

Broadly, the system may be divided into five sub-systems, each of which may be further divided into a number of fuctional groups which, in turn, may each comprise one or more instruments. Sub-systems and major groups are:

Sub-Systems	Groups
Geophysical	Seismic Gravity Magnetic
Navigation	Sonar Doppler Velocity log Gyrocompass VLF
Oceanographic	Water temperature and salinity
Atmospheric	Wind velocity Air pressure, temperature, humidity
Data Acquisition	Timing Analogue-to-digital conversion Digital-to-analogue conversion Data processing and multiplexing Digital input/output peripherals Chart recorders

It is anticipated that only the data acquisition sub-system (DAS) will be supplied by BMR, the remainder being hired with the survey vessel. We therefore have complete control over the DAS configuration, but must take what the contractor provides for the other sub-systems. As it would be impracticable and uneconomical to postpone interfacing considerations until after the contract is awarded, it is necessary to devise a flexible interfacing system able to accommodate any likely instrument configurations. In devising such a system, it is extremely important to follow the general recommendations of the foregoing sections in order to avoid the system hazards inherent in an unspecified environment.

Considerable thought and expense have ensured that the DAS is provided with a number of fail-safe and data-checking features designed to guard against loss of data and poor-quality data; these efforts could be wasted if data quality is jeopardized by unsound interfacing to the DAS.

7.2 Analogue Interfacing

This is straight-forward: most, if not all, analogue channels require amplification and/or filtering. A prototype amplifier/filter has already been designed and constructed in the

BMR laboratories - file 75/53. This unit, designated TAM7, is designed to plug into a ruggedized bin also of BMR design. The bin is a standard 5¼ inch x 19 inch rack-mounted unit, with plug-in power-supply module, and able to accommodate up to eight TAM7 modules. The bin has a rear panel grounding link as mentioned in Section 3.7, and should be located as close as possible to the analogue source.

Although the TAM7 output is single-ended, a separate ground connection is available for each module. Differential connection can thus be made to the analogue/digital converter. Full-scale signal swing is ± 10 volts. A second identical, but isolated, output is available from each TAM7 for direct connection to a chart recorder, so that data can be recovered if the digital system fails.

7.3 Digital Interfacing

This is complicated by the large number of unknowns in the vessel installation. A perfectly general system requires a sending interface unit to acquire the data, optically isolate it, and drive the line to a receiving interface unit which presents the data in the required form to the DAS.

7.3.1 Sending Interface

It is necessary to list the unknown factors of relevance in acquiring digital data as an aid to devising a "universal" interface. The following list of questions is illustrative:

1. What logic family is used at the output of the source instrument? Is it TTL, LPTTL, HTTL, DTL, LPDTL, MOS, CMOS, RTL, CTL, discrete, relay contact or other?

2. What are the voltage levels corresponding to high and low logic states, and what loading is permissible? Are one or both states negative?

3. Is the logic convention negative- or positive-true?

4. Is the logic code BCD, binary, or other?

5. Is the data latched, and if so, is a "busy" line provided?

6. Is the data transmitted differentially, single-ended with ground return, or single-ended single-wire?

7. Is a shunt terminating resistor required, and if so, what value?

8. If single-ended, is a switching threshold reference voltage provided, or if not, is access to internal supply voltages provided so that such a reference can be derived?

9. Can turn-on/turn-off transients exceed the normal logic levels?

Considering each of these questions in turn helps to specify the input requirements of the sending interface unit.

A device having high input resistance and high differential and common mode input voltage ranges (including negative values) will satisfy the alternatives in questions 1 and 2.

If the device is differential and the inputs can easily be reversed, question 3 no longer matters.

Software arrangements in the DAS take care of question 4.

Question 5 ultimately poses the most problems: If the data is not latched, a latch can be provided in the receiving interface unit where it can be gated by the DAS. However, there can be no guarantee that such asynchronous operation will always ensure valid data. If the data is latched but there is no "busy" line, a similar problem exists. Thus unless the source instrument has both latch and "busy" line, there is always a possibility (usually very low) of invalid data when the instrument is sampled asynchronously by the DAS. Provision for synchronous sampling does not exist on many instruments. It seems that without resorting to undue complexity the best that can be done is to provide a latch in the receiving interface which will at least ensure that the data is not changing when sampled.

To satisfy the alternatives posed by question 6, the input connection should be a differential two-wire transmission line with optional provision for earthing one side. Another option should allow one side of the input device to be connected to a suitable reference voltage. Even if the source has only a single-wire output, a twisted pair can be used at least as far back as the connector, where the return lead can be grounded or connected to a reference voltage if provided.

Questions 7 and 8 are taken care of by making provision for an optional terminating resistor and providing a voltage divider network which, in the event of single-ended operation with no reference voltage, can be connected either externally to the source voltage supplies, or internally to the interface supplies, thus providing a reference.

Protection against excessive differential and common mode input voltages satisfies the final question.

The input device, which will probably be some form of line receiver, should be able to drive the input of an opto-isolator and should settle quickly to avoid ambiguities in the data output.

A power supply must be provided for the line receiver. This should be mains operated with high isolation and a floating ground which should be returned to the ground of the source group.

The ground reference for the opto-isolator output and line driver must come from the receiving interface. The power supply for these devices must also be referenced to this ground, thus demanding either a completely independent +5 volt mains-operated supply, located in the sending interface bin, or a +5 volt regulator in the sending interface supplied by a higher dc voltage from the receiving interface. (Use of a regulator at the sending interface will reduce noise which could be picked up if the +5 volts were supplied direct from the receiving interface bin.) The second of these possibilities provides better ground isolation and is therefore favoured.

The questions of the optimum numbers of data bits per module and modules per bin must also be examined. The digital multiplexer in the DAS accepts 12-bit words. Thus, for a simple one-to-one interconnection system between each interface and the DAS, 12 data bits plus one "busy" bit per module seems reasonable, giving 3 BCD digits per module. This is also likely to provide a reasonable component density.

Because the bins need to be close (preferably within 1 metre) to the source instruments, there is no point in having many modules to a bin if the locations of the source instruments are even moderately distant. Dividing the source instruments into likely groupings indicates that four modules per bin is probably optimum. Generally, each module in a bin will connect to the same source group, so there will be no earth loop problem if only one plug-in power supply is used to power all input circuits. However, if there is room in the bin, complete isolation can be ensured for relatively little extra cost by providing each module with its own mains-operated supply.

The +5 volt regulators for the output circuits should probably be separate for each module and located within the module.

Figure 4 summarizes the requirements for the sending interface. It is not intended as a final circuit but as a starting point. Where device types are indicated, they are only intended to characterize the device and are subject to alteration by the detail designer.

The high-value resistors shown from the line receiver inputs to the supply rails ensure that a definite condition, namely logical "1", appears at the sender output if the input is disconnected. This condition, which could indicate a cable fault, is more likely to be detected in a BCD code than logical "0", and it is better to have a definite logic level than some random effect due to a floating input. These resistors will also enable the sender to operate from relay contact closures in the source instrument.

For consistency and ease of servicing, it is recommended that the positive-true logic convention be adopted for all data interconnections. It should be noted, however, that negative-true logic is often used between a computer and its peripherals, and these should be interfaced as intended by the manufacturers.

The bin for the sending modules should be grounded only through its mounting and bonding; because of the possibility of up to five different ground lines associated with the sending modules, it is preferable not to connect the bin to any of them.

7.3.2 Receiving Interface - General

The requirements for the receiving interface are greatly simplified by the normalizing of data by the sending interface, and are:

1. Supply of power to the associated sender.

2. An input gate to act as a line receiver for each incoming line. This gate should have a pull-up resistor to give logical "1" if the input is disconnected.

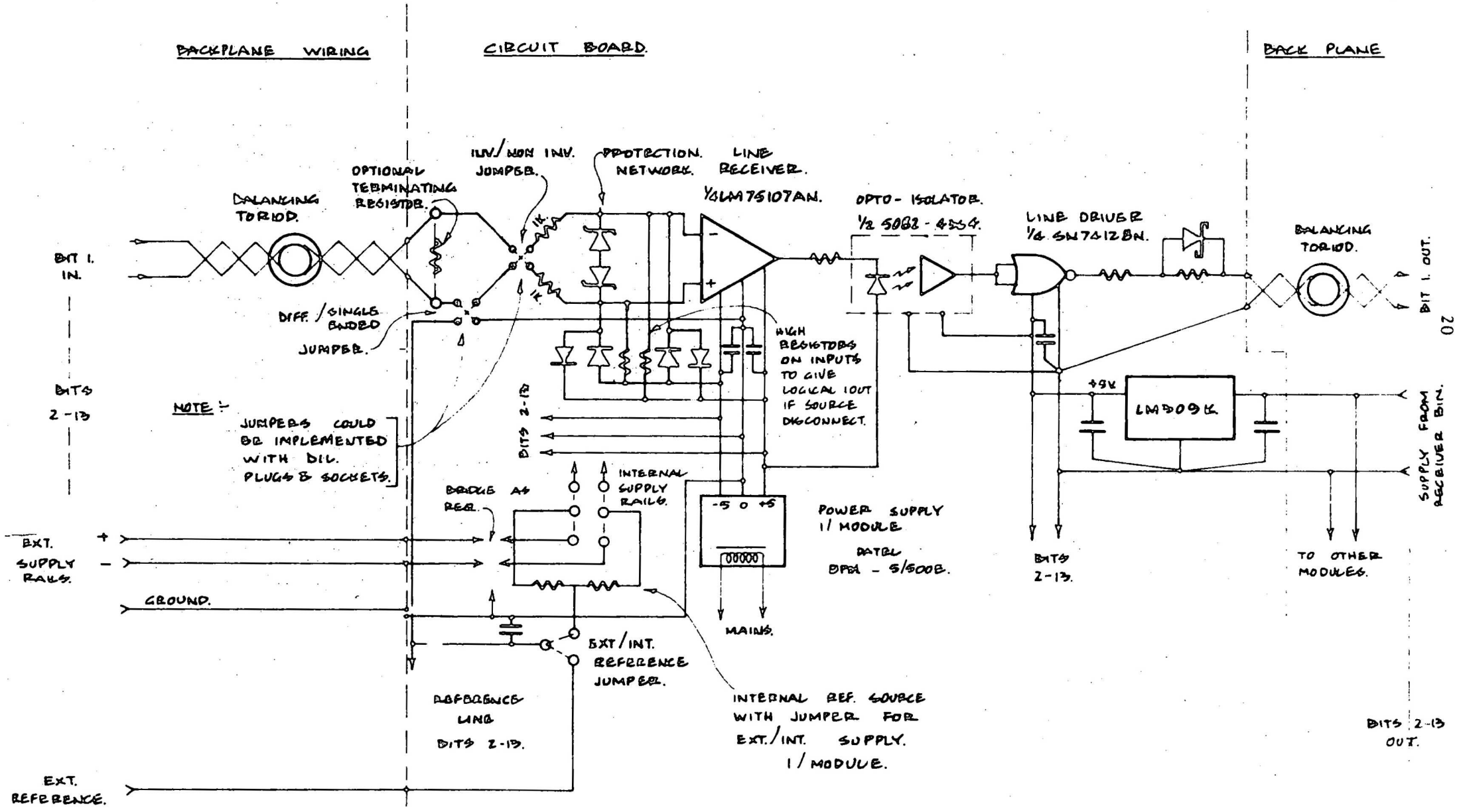
3. A latch for each bit, capable of interacting with both the "busy" line from the source and the control lines from the DAS multiplexer.

4. An output line driver gate to drive each data line to the multiplexer. Because the multiplexer to be used requires positive-true logic, both the line receiver and line driver gates should either be inverting or non-inverting, assuming no inversion through the latch.

5. A second output line driver gate for each bit, providing a positive-true signal for the digital-to-analogue converter (DAC) used to produce back-up chart records. This second output gate should take its input before the latch, in order to keep the

FIGURE 4: SENDING INTERFACE REQUIREMENTS.

(CIRCUIT INDICATED FOR ONE BIT ONLY)



back-up monitoring system safe in the event of a DAS malfunction. However, to allow for the possibility that the data source has no latch, an optional hard-wired connection to the latch output is desirable. There is no need for either power or speed in the drive to the DAC, but maintenance would be simplified if both DAC and DAS drive gates are of the same type.

Bin configuration is simpler than for the sending interface, as a common ground can be used for all circuits. A 12-bit module will permit a one-to-one interconnection to both the sending interface and the multiplexer. A common power supply can be used for all modules - and those in the associated senders. An optional grounding link can therefore be provided to connect circuit ground to the bin. It is likely that at least eight 12-bit modules will fit into one bin with power supply.

Figure 5 summarizes the requirements for one BCD digit (four bits).

The control circuitry indicated in Figure 5 ensures that fresh data can enter the latch only when requested by the DAS; it also ensures that the latch contents are updated in the event of an overlap of the DAS gate signal and the device "busy" signal - a distinct possibility with asynchronous operation. The requirements for this circuitry are discussed in Section 7.3.4 where the multiplexer operating mode is considered.

The omission of reverse termination at the DAS drivers is a consequence of the input circuits used in the Hewlett-Packard multiplexer: there must be either a pull-up resistor or a voltage divider on each input gate. The effect, in either case, would be to degrade excessively the logic low level obtained with reverse termination. The network used by Hewlett-Packard does mitigate some line driving problems, however.

The receiving bins are expected to be located close to the DAS, so that high-powered line driving gates are unnecessary. Standard 7400 series gates should be satisfactory, provided normal precautions are maintained. The same applies to the DAC driving gates which can be reverse terminated - a requirement which, in this case, is not so necessary for signal fidelity as for keeping self-generated ground noise to a low level.

If desired, logic inversion can be obtained by direct substitution of an SN7408 for the SN7400.

The following section discusses features, included in Figure 5, which are not required for driving the multiplexer, but necessary for interfacing to other DAS inputs. Whether a special interface is used for the latter requirements, or a single general-purpose interface is used, is up to the detail designers.

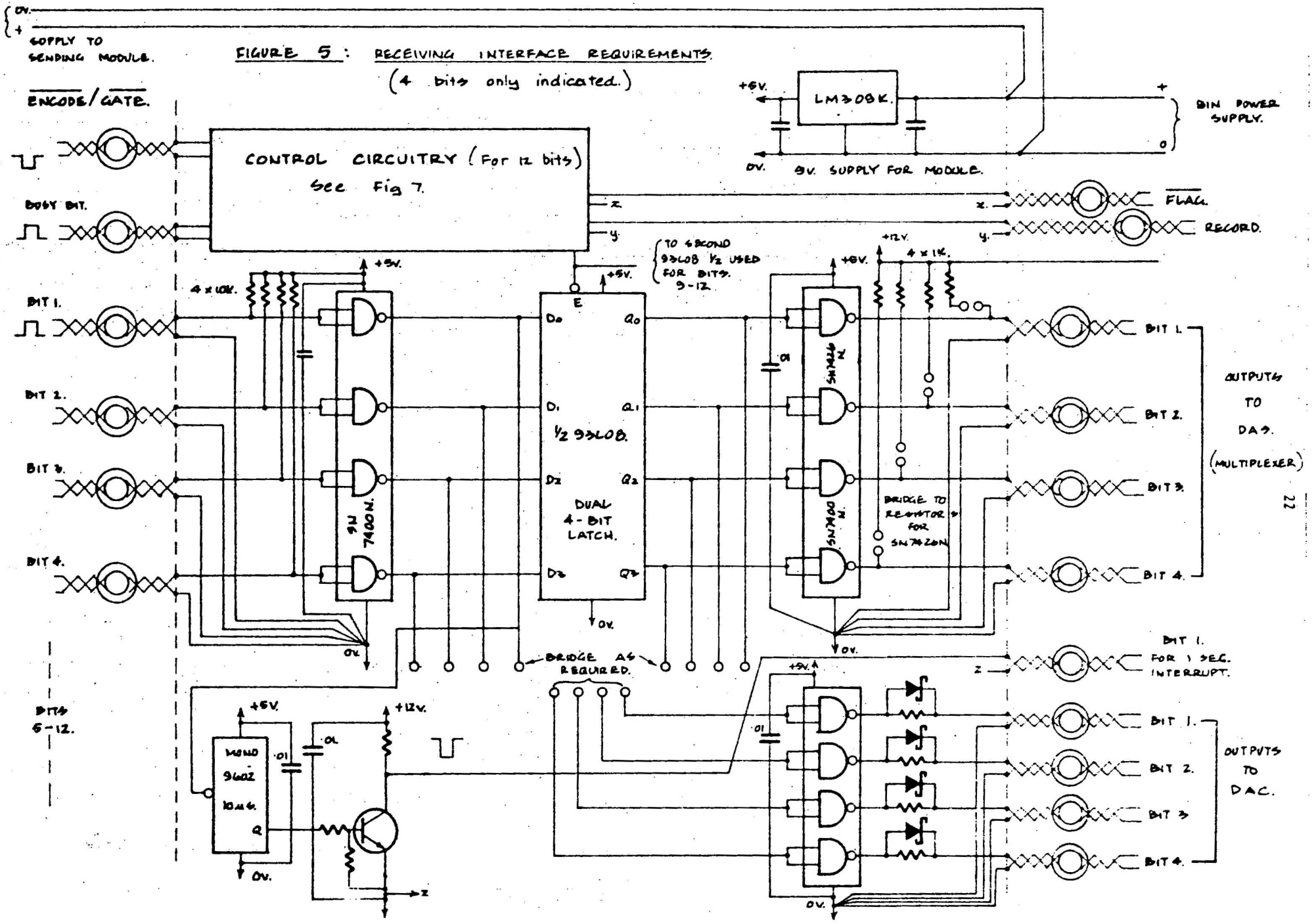


FIGURE 5 : RECEIVING INTERFACE REQUIREMENTS.
(4 bits only indicated.)

7.3.3 Receiving Interface - High Level Output

Time information from the two system clocks is not multiplexed but is input directly to the computer via 32-bit general-purpose data-source interface cards: Hewlett Packard type 12604B. These cards differ from the multiplexer cards, both in their control signal requirements and in the voltage levels for input data: logic "1" should be 5 to 100 volts more positive than logic "0" within a window of -100 to +100 volts. In addition, a reference voltage 0.5 volt less positive than the logic "1" level is required.

It is therefore recommended that an open collector driving gate be used (SN7426) with pull-up resistors to a +12 volt supply. (Note that this device can be directly substituted for the SN7400). Receiving bin number 1 on the system block diagram is the only bin requiring this supply, but again, in the interests of uniformity, it may be better to have a single universal receiving bin design. In either case, the two reference lines required from the bin could simply be obtained from a forward-biased diode connected to the 12-volt line, giving approximately 11.5 volts reference.

A further unique requirement from bin number one is for one bit, an unlatched pulse to provide one-second interrupts, to interface with a 16-bit duplex register, Hewlett Packard type 12554A. This register requires a logic "1" level of zero volts and a logic "0" level of +8 to +12 volts. Figure 5 shows a 10-microsecond monostable and transistor driver to meet this requirement; no control lines are needed to input this bit, as it has over-riding priority.

7.3.4 Control Circuitry for DAS Interfacing

As mentioned above, the receiving bins must interface with either:

1) the multiplexer, a Hewlett Packard multiprogrammer, model 6940A, with digital input card model 69431A, option 073 (positive-true TTL input levels)

or 2) 32-bit general-purpose data-source interface card, Hewlett Packard type 12604B.

The control requirements for each of these will be summarized in turn and a circuit approach recommended.

The 69431A digital input card initiates a request for data by a negative-going transition on its GATE line, hereafter termed the gate line. This transition tells the data source that fresh information is required, and the data source in turn is

expected to respond by applying a negative-going transition to the FLAG line, hereafter termed the flag line. This transition tells the 69431A that a measurement is being performed, or data refreshed, etc., and causes the gate signal to reset to its high state. (Note that an internal jumper option allows the gate to be reset on the trailing edge of the flag signal if desired.) At the conclusion of the measurement process the data source is expected to return the flag line to its initial high state, thus informing the 69431A that the required data is present on its input lines. The data is expected to remain on the input lines for at least three microseconds after the positive flag transition. An additional, but minor, constraint is that the flag signal must rise and fall at a rate greater than 0.1 volts per microsecond.

The operation of the 12604B is slightly different. A number of options may be employed for various input sources, but only those relevant are discussed. The data request is initiated by a negative-going transition from +13.5 volts to zero volts on the ENCODE line, hereafter termed the encode line. The data source does not respond until the measurement is complete, at which time the data source is expected to pulse the RECORD line, hereafter termed the record line, with a positive pulse of 4.5 to 20 volts amplitude and a minimum duration of 20 microseconds. On receipt of this pulse the encode line is restored to its initial high level and, after an optional delay time of 1 millisecond or 0.1 millisecond to allow data to settle, a pulse is generated to inform the computer that data is ready. (A settling delay time of 0.1 milliseconds is recommended for this application). Unlike the 69431A, the 12604B has no data storage register, so the data should remain unchanged until the next encode pulse occurs.

If the internal jumper in the 69431A is wired to reset the gate line on the trailing edge of the flag signal, the two interfaces operate similarly as summarized in Figure 6 (ignoring level differences).

In the present application, the measuring period indicated in Figure 6 is the time for which the hold signal is removed from the latch in the receiving interface, thus allowing fresh data to enter. The situation is complicated by the "busy" signal transmitted asynchronously by the source instrument. If this is present when a gate/encode command is received, the latch hold should not be removed until after the "busy" signal terminates. If a "busy" signal arrives while the latch hold is removed, the latch hold should stay removed until after the "busy" signal terminates. Arrival of a "busy" signal at any other time should have no effect. The flag signal can then be derived from the latch hold signal and the record signal from the trailing edge of the flag signal.

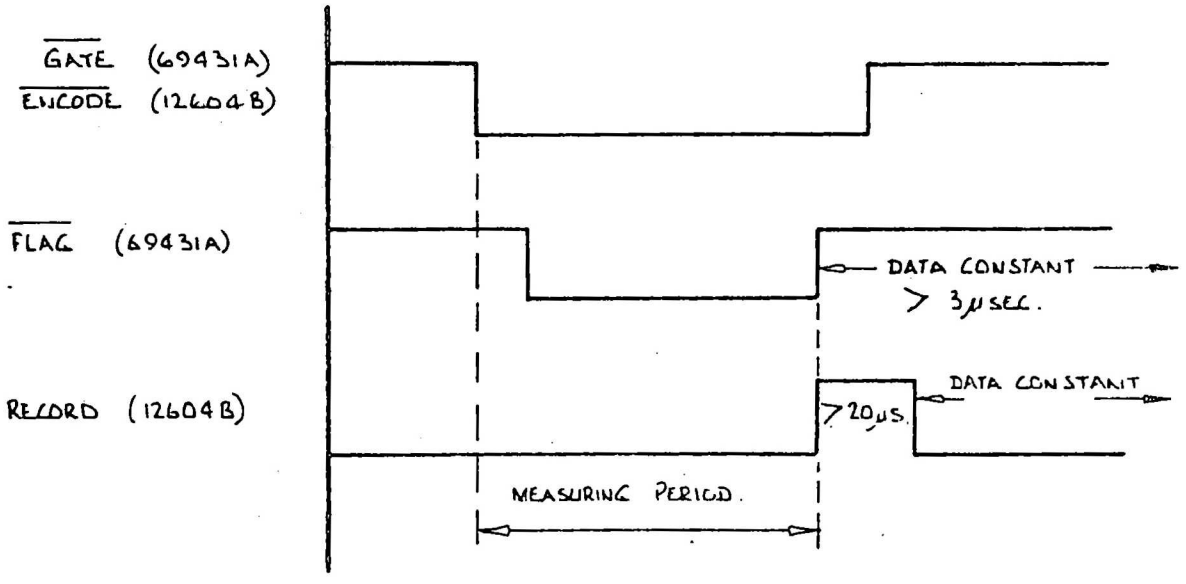


Figure 6. Interface Control Sequence.

The schematic of Figure 7 suggests a control circuit (one per receiving module) intended to fulfil all requirements for either interface.

The transistor input stage on the gate line should also accept the encode signal, normalizing both to logic level. A transistor output stage operating from +12 volts provides the required levels for the record signal. An RC network is used to gate both the record and flag signals to ensure that spurious operation of the monostables on turn-on does not give unwanted output. The network should disable the outputs for a time greater than the sum of both monostable periods.

The following four situations are depicted in the waveform diagram:

A. Busy signal only: no effect

B. Gate signal only: a 20-microsecond flag and latch hold pulse followed by a 50-millisecond record pulse.

C. Gate signal occurring while busy signal on: flag and latch enable produced on receipt of gate and extending for 20 microseconds after busy signal

ends. Note that an unwanted spike is possible in flag signal when monostable turns on. An RC circuit having a time constant of about one microsecond has been included in the circuit to eliminate this.

D. Busy signal occurring while gate signal on: flag and latch hold extended for duration of busy signal plus 20 microseconds. As before, unwanted spike is possible unless busy signal terminates within 20 microseconds of start of gate.

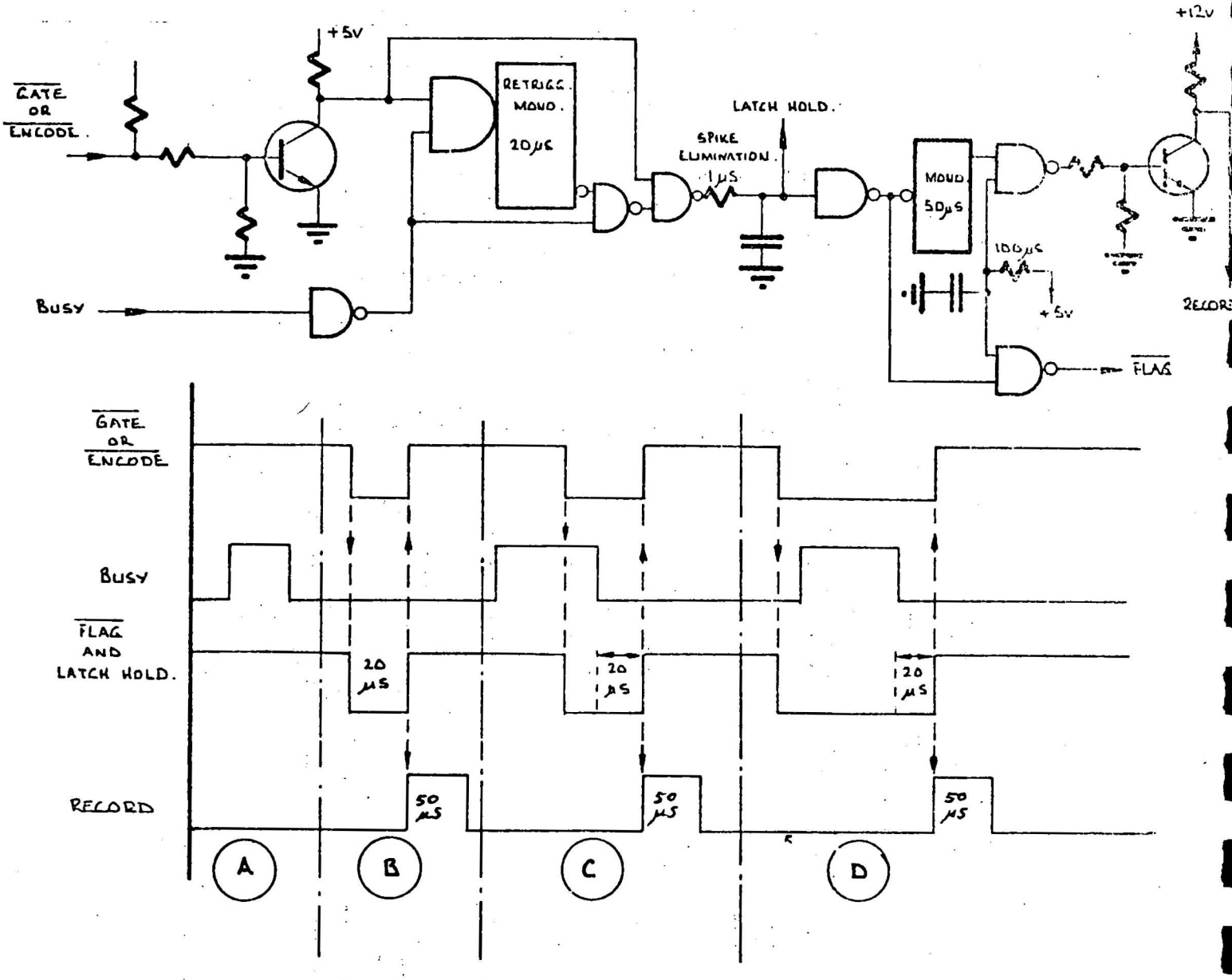


Figure 7. Control Circuit and Waveforms

It is apparent from the system block diagram that more than one 12-bit module can be associated with the one source instrument. Provision must therefore be made for the gate signal first applied to such a module group to latch the data on each module in the group simultaneously, to ensure that all 12-bit words acquired relate to the same reading. Gate signals applied to subsequent modules in the group should only return a flag signal without operating the latches. This can be achieved simply by the use of toggle switches, mounted on the bin rear panel (or internally) as shown in Figure 8.

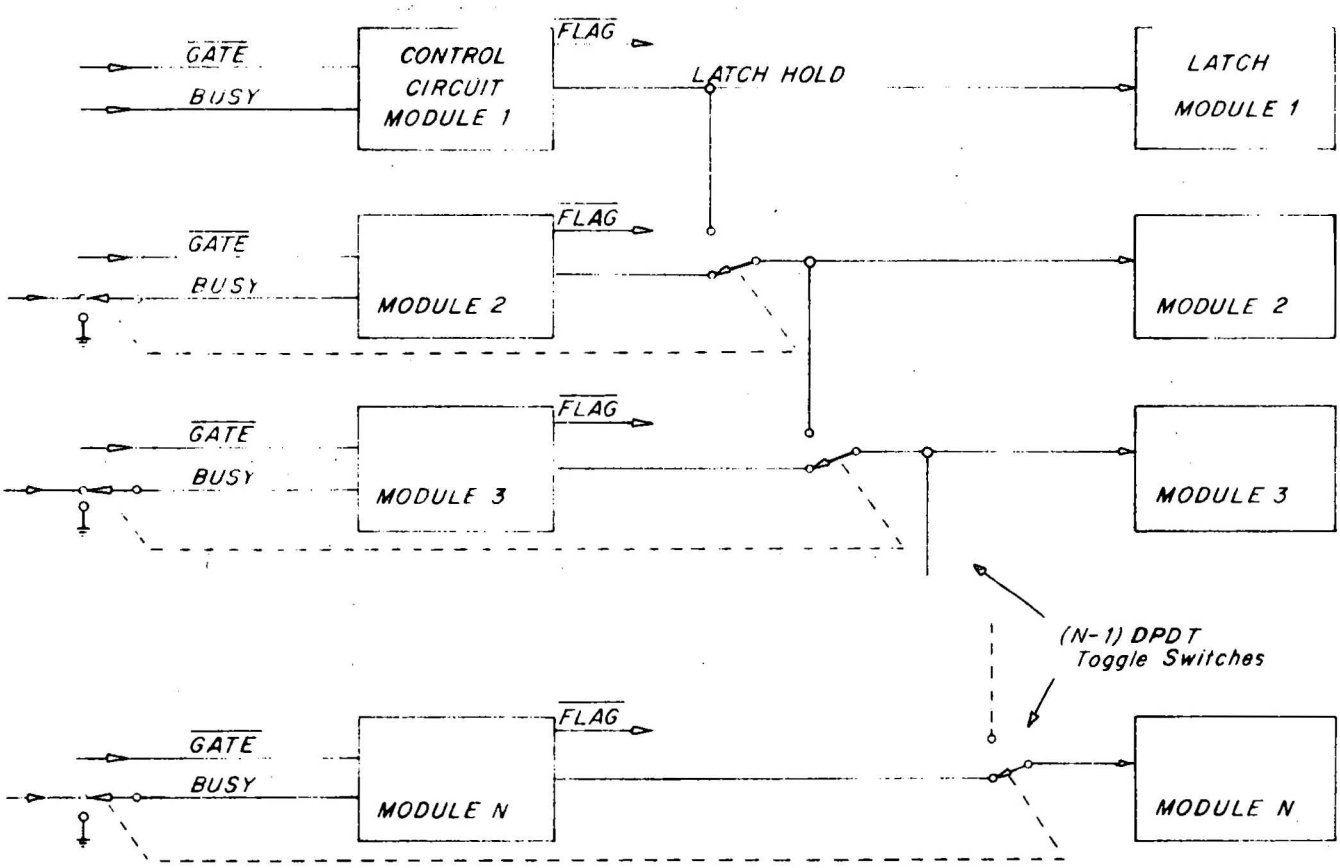


Figure 8. Circuit for Common Latching

8. Conclusion

Various aspects of equipment interfacing have been discussed, with particular reference to interfacing digital signals to the data acquisition system for the 1977 marine survey. If the recommendations made are followed, very little trouble should be experienced in connecting to any source

instrument likely to be offered by the contractor. Ignoring the recommendations could mean many man-weeks of trouble-shooting and ad hoc problem solving, possibly while the vessel is on charter. The estimated $33 000 needed to construct interfacing equipment is therefore a worthwhile insurance.

Although it has been necessary to illustrate various points with detailed circuits, these are not necessarily final, as the detail designer may encounter unforeseen problems or devise a more efficient approach.

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HEWLETT-PACKARD OPERATING AND SERVICE MANUAL, DEC 1971 - Digital input card Model 69431A, HP Part No. 69431-9000.

HEWLETT PACKARD OPERATING AND SERVICE MANUAL, 1970 - Data source interface 12604B, HP Part No. 12604-90002.

APPENDIX

Summary of Frequently Used H-P Interface Units

A.1 Introduction and General Interface Description

In dealing with interfacing requirements for the Hewlett-Packard mini-computer, Section 7 of this record briefly covered some aspects of the particular types of computer interface necessary to implement the system proposed at the time of writing. Because of the possibility of changes occurring as the system evolves, it is considered desirable to list more fully the characteristics of all H-P interfaces likely to be used for data acquisition. Interfaces designed for a specific peripheral, such as a paper tape punch, magnetic tape, etc. will be omitted. Full details of all interfaces may be found in the appropriate operating and service manuals.

The Hewlett Packard publication "A Pocket Guide to Interfacing the HP2100 Computer" gives a concise description of most aspects of interfacing. This appendix, while duplicating some of this information, is primarily concerned with the hardware aspects of interconnection and "black box" operation of specific units. Additional information is therefore drawn from the interface operating manuals. Line driving waveforms are derived theoretically via Bergeron diagrams.

A computer interface is a circuit for transferring data between the computer and an external instrument (I/O device), under programme control. Each interface takes the form of a circuit board which plugs into an addressable slot in the computer mainframe. Connection to the I/O device is via an edge connector on the outer edge of the board. There are two main sections in an interface: data input/output circuits, possibly including temporary storage registers, and control circuits to initiate and synchronize the data transfer and to supply the necessary address, priority, and interrupt signals. Both data and control circuits must be compatible with the inputs and outputs of the I/O device, a variety of interfaces being necessary to handle the wide ranges of voltage, impedance levels, data transfer speeds and logic conventions in general use.

Usually there are at least two control lines between the interface and I/O device: the device flag line allows the device to signal to the computer that input data is ready to transfer, or that output data has been accepted. The device command line (also termed the gate line or encode line) allows the computer to signal to the device that input data is requested, or that output data is ready to transfer. Either or both of these lines may be necessary in some simple applications. Additional control lines may be necessary when interfacing to complex peripherals such as a teleprinter or magnetic tape unit.

To appreciate some of the interface options available it is necessary to understand the operation of part of the control logic used to generate an interrupt request (IRQ) - a request

by a particular interface for service. Figure A.1 is a very simplified logic diagram which omits all logic concerned with addressing, priority, resetting, and synchronization with the computer timing cycle.

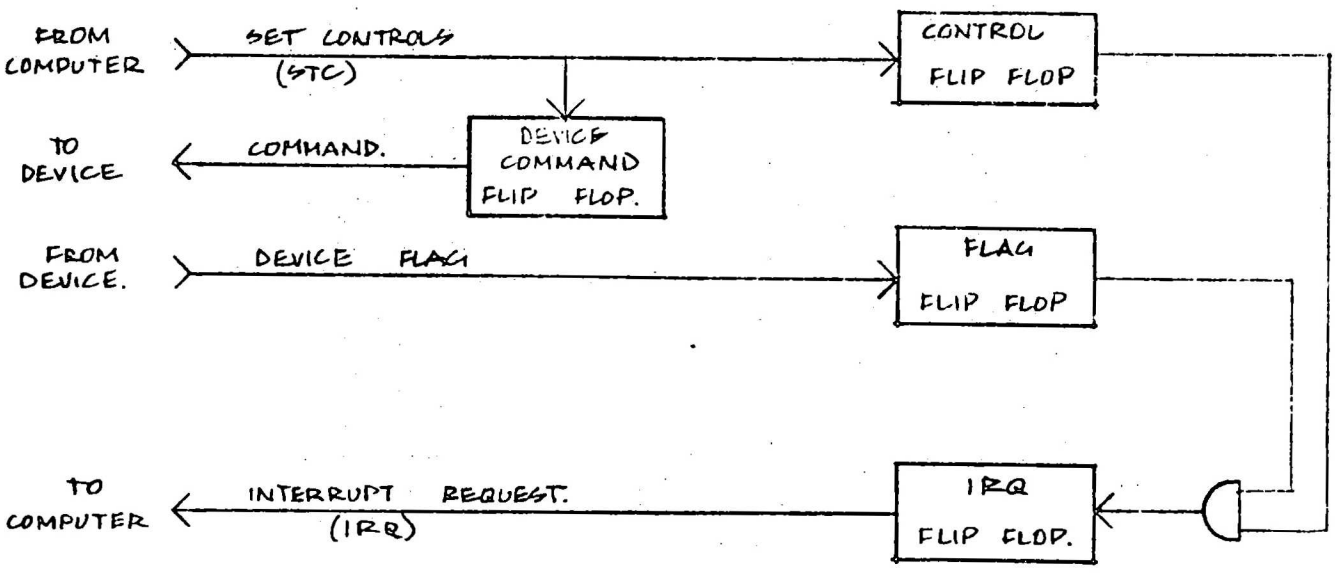


Figure A.1 Simplified IRQ Logic

An I/O timing cycle for the 2100 computer consists of five periods, each of 196 nanoseconds duration, designated T2 to T6. This designation maintains compatibility with the earlier 2114, 2115, and 2116 computers which had eight periods, TO to T7 in their I/O timing cycles.

At time T4, a set control (STC) instruction sets the control flip flop and the device command flip flop, thus issuing a request for data or notifying the I/O device that output data is ready. When the I/O device has responded - possibly many cycles later - it will supply a flag signal causing the flag flip flop to set at time T2 of the next cycle. Outputs from both the control and flag flip flops are "anded" to enable the interrupt request flip flop which sets at time T5. The request will be serviced (the computer informed that input data is ready or that output data has been transferred) in the next or subsequent timing cycles, depending on whether a higher priority device has generated an interrupt. On input operations the device flag signal may be used to strobe data into temporary storage registers on the interface card when such storage is supplied.

Most interfaces have a number of user selectable options, e.g. data storage/non storage, positive-negative-going control signals. The appropriate operating manual should be consulted to

ensure that the correct options have been selected for each application. Details of input/output voltage levels and circuits, as well as control signal requirements are necessary for interfacing, and will be given in the following sections.

A.2 Interface Characteristics

The characteristics to be listed are taken from the latest information available. There could be slight discrepancies when applying this information to cards not incorporating the latest design revisions. Such discrepancies should not be serious because of the manufacturer's philosophy of downwards compatibility in the implementation of design improvements.

Interfaces to be specifically considered are

1. Microcircuit Interface 12566B
2. 16-Bit Duplex Register 12554A
3. General Purpose Date Source Interface 12604B
4. Digital Input Card 69431A for Multi-programmer

A.3 Microcircuit Interface Type 12566B

A.3.1 Application

This interface is intended for use with I/O devices having DTL or TTL logic levels. It has independent 16-bit input and output storage registers, but only one flag control circuit which can therefore only be associated with an input or an output operation at any one time. The maximum possible data rate for the basic interface, unlimited by processor speed, is 600,000 16-bit data transfers per second. Such rates can only be approached when the interface is coupled through the Direct Memory Access (DMA) section of the computer.

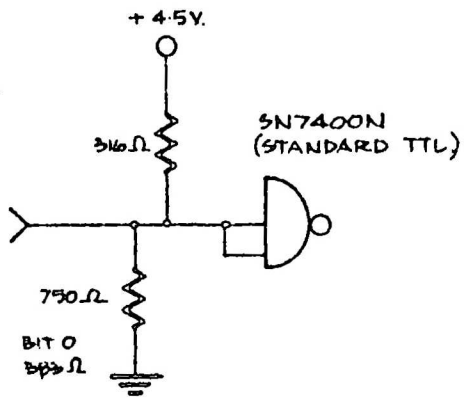
A.3.2 Factory Variations

Type 12566B	:	Ground-time logic. Outputs are "wire-or" tieable.
Type 125668-001	:	Same as basic type but connector supplied connects outputs and inputs together for pulsed party-line configuration.
Type 12566B-002	:	Positive-time logic. Outputs are not "wire-or" tieable.
Type 12566B-003	:	Same as basic type but consists of circuit board only, without connection kit and cable.

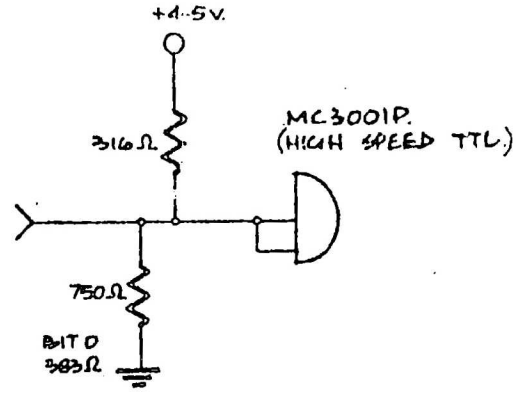
A.3.3 Specifications of Input and Output Circuits

SIGNAL CONDITIONS		GROUND-TRUE MICROCIRCUIT INTERFACE P/N 12566-60024		POSITIVE-TRUE MICROCIRCUIT INTERFACE P/N 12566-60025	
		"0" LEVEL	"1" LEVEL	"0" LEVEL	"1" LEVEL
DATA AND FLAG INPUTS	VOLTAGE	+2.4 TO + 5V	0 TO +0.5V	0 TO +0.5V	+2.4 TO +5V
	BIAS AND IMPEDANCE	BIT 0: +2.5, 174 OHMS; OTHERS: +3.2V, 222OHMS			
	CURRENT REQUIRED	-	-15 mA	-15 mA	-
DATA AND COMMAND OUTPUTS	VOLTAGE	+2.4 TO +5V	0 TO +0.5V	0 TO + 0.5V	+2.4 TO +5V
	IMPEDANCE	1 k OHM	LOW	LOW	APPROX 100 OHMS
	CURRENT SINK	-	31 mA (MAX)	31 mA (MAX)	-

Input Circuits

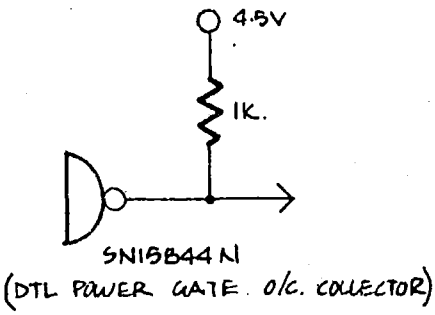


GROUND-TRUE DATA AND FLAG
POSITIVE-TRUE FLAG

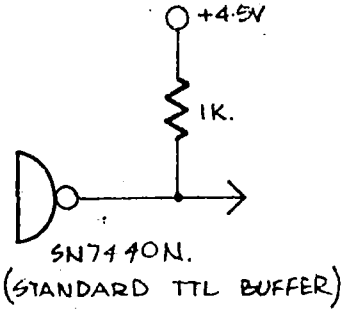


POSITIVE-TRUE DATA

Output Circuits

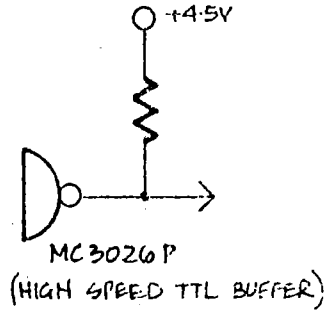


GROUND-TRUE DATA



GROUND-TRUE COMMAND

POSITIVE-TRUE COMMAND



POSITIVE-TRUE DATA

The input circuit bias network automatically ensures a high logic level if the input is open circuited. Thus logic high may validly be obtained from a source which merely assumes a high impedance, provided that such a circuit can withstand a potential of up to +5 volts.

The ground-time data output circuit is the only output circuit using an open circuit collector gate, and hence the only circuit which can be used in the "wire-or" configuration.

A.3.4 Line Driving and the Microcircuit Interface

When driving an input circuit from a long line, the input bias network precludes reverse termination because the voltage dropped across the reverse termination resistor in the logic low state would elevate the input circuit voltage to a level in excess of the +0.5 volts specified. However, the bias network provides a certain amount of short termination which, although not ideal, does have the effect of shifting the steps on the voltage wave-form away from the threshold level, thus providing better noise immunity than obtainable from an unterminated line.

Figure A.2 shows typical waveforms to be expected when driving an input circuit via a long 80 ohm line from a standard TTL gate (SN7400N) and a TTL line driver (SN74128N).

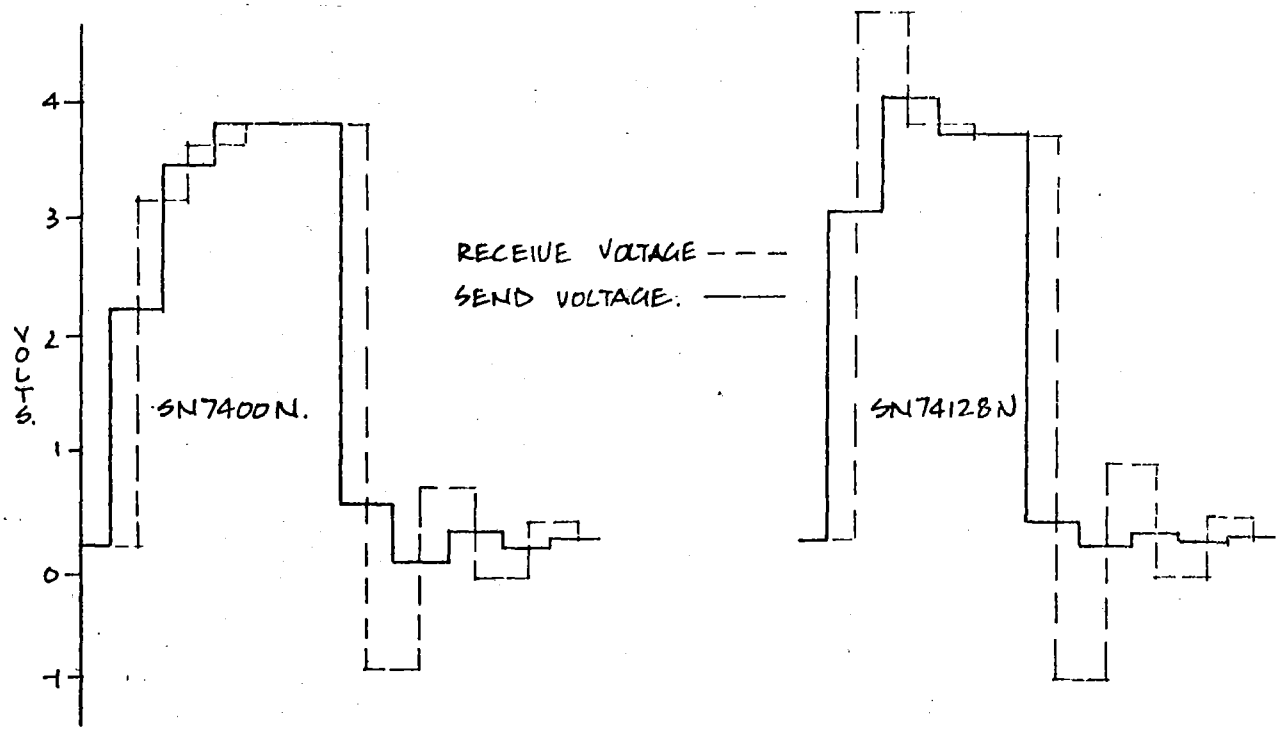
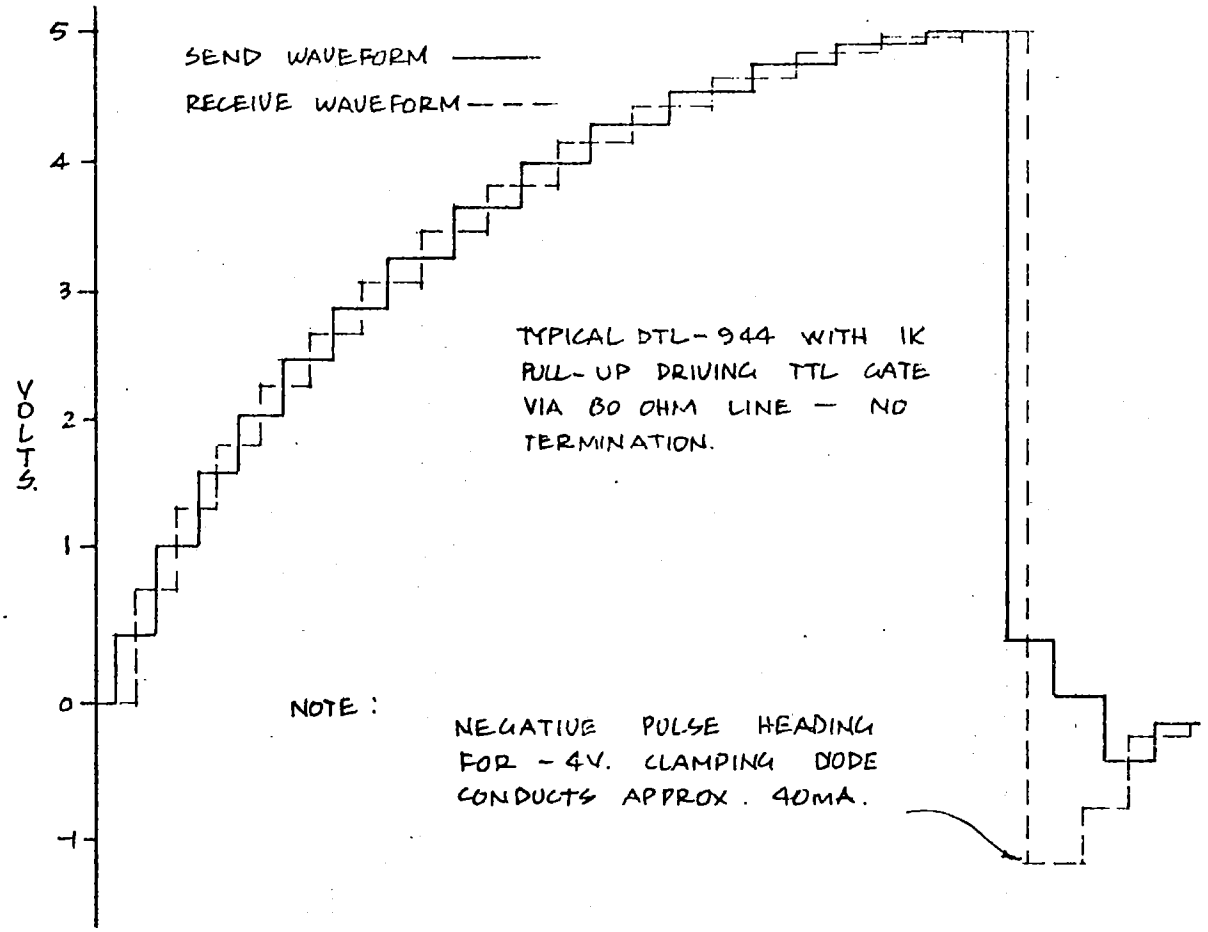


Figure A.2 Line Driving Microcircuit Inputs

Figure A.3 depicts typical waveforms to be expected when driving TTL gates from the ground-true data output circuits via an 80 ohm line. Waveforms are shown for no line termination and for the voltage divider termination as used on the input circuits. Hewlett-Packard's recommendation to use this form of termination is clearly justified, especially when the DTL driver drives to the high level. Where high noise immunity and fast settling are important the positive-true interface option is preferable; with voltage divider termination, its output waveforms should lie between the two cases shown in Figure A.2. The waveforms from the device command outputs, for either option, should be similar to those from the positive-true data outputs.



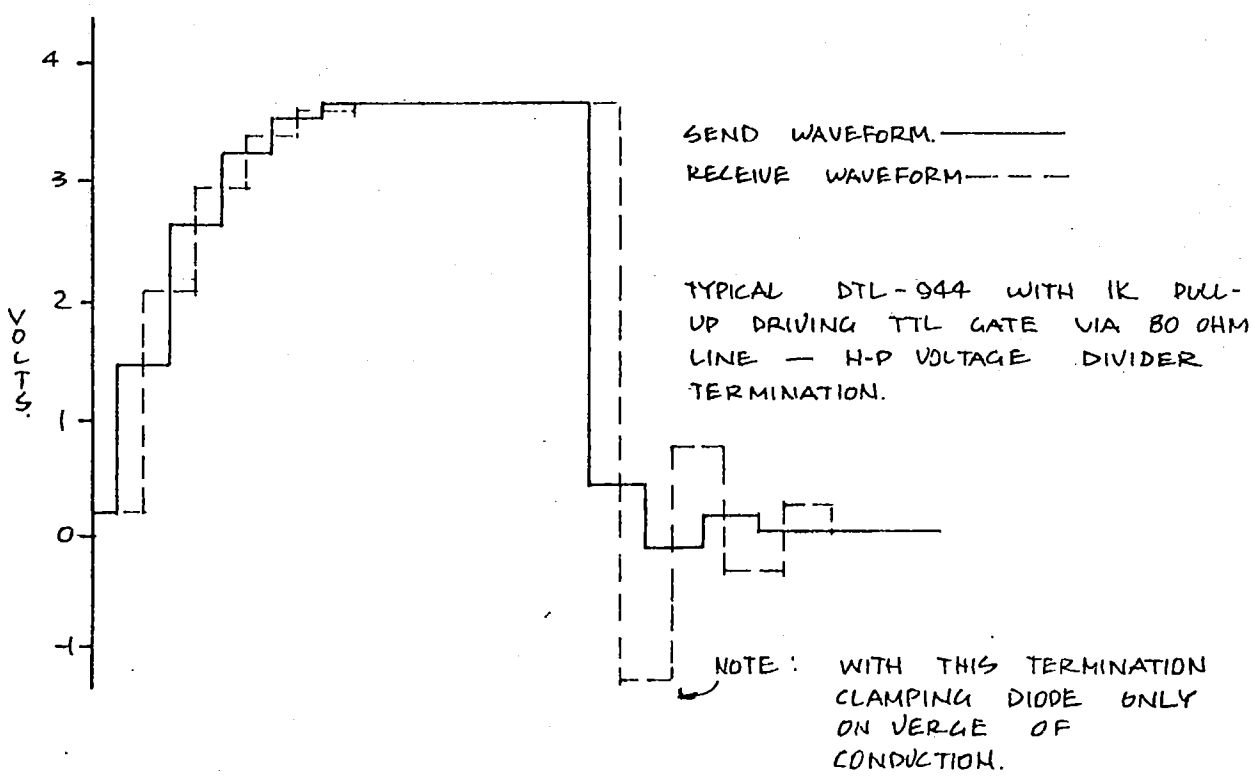


Figure A.3 Line Driving from Microcircuit Ground-True Outputs

A.4 16-Bit Duplex Register Type 12554A

A.4.1 Application

The 16-Bit Duplex Register is very similar to the Microcircuit Interface, the Major difference being the input/output voltage levels: 12 volt transistor circuits are used rather than DTL/TTL compatible circuits. Maximum possible data rate for the basic interface, unlimited by processor speed, is 100,000 16-bit data transfers per second.

A.4.2 Factory Variations

Type 12544A : Positive inputs and outputs

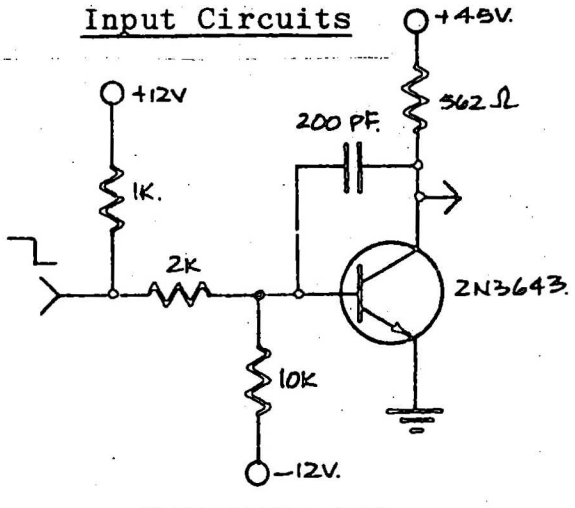
Type 12544A-002 : Negative inputs and outputs

The logic convention for both types is negative-true, the distinction being one of actual voltage levels.

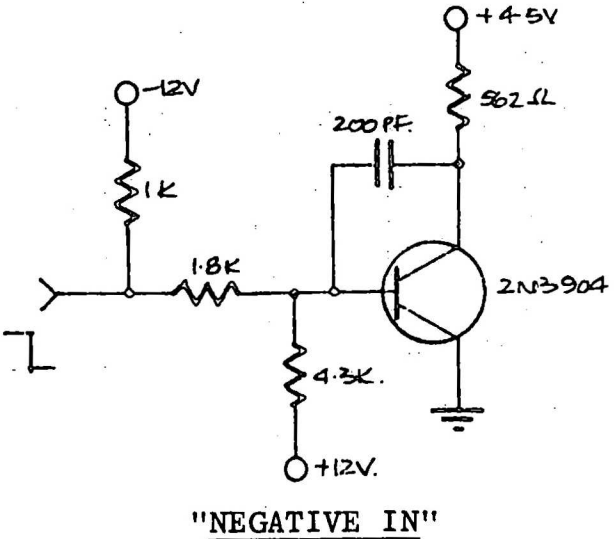
A.4.3 Specifications of Input and Output Circuits

SIGNAL CONDITIONS	POS. IN/POS. OUT DUPLEX REGISTER P/N 12554-60023		NEG. IN/NEG OUT DUPLEX REGISTER P/N 12554-60024	
	"O" LEVEL	"1" LEVEL	"O" LEVEL	"1" LEVEL
DATA AND FLAG INPUTS	OPEN CIRCUIT OR +8V @ 0 mA TO +12V @ +5 mA	OV TO +0.5V @ -12 mA	OV TO -0.5V @ +12 mA	OPEN CIRCUIT OR -8V @ +0.7 mA TO -12V @ -4 mA
DATA AND COMMAND OUTPUTS	+12V FROM 10K RESISTOR	OV TO +0.5V 12mA SINK MAX	OV TO -0.5V 12mA SOURCE MAX	-12V FROM 10 K RESISTOR

Input Circuits

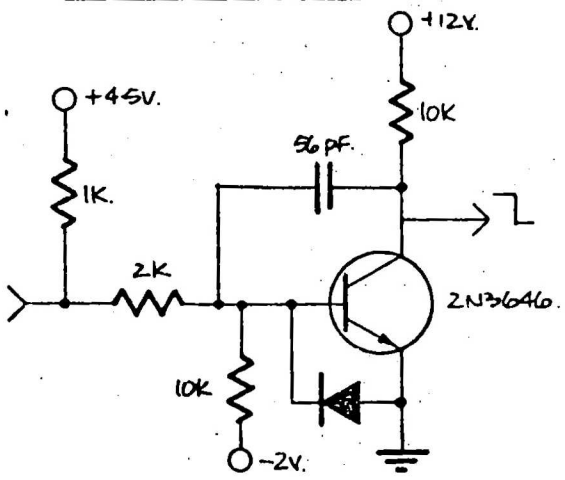


"POSITIVE IN"

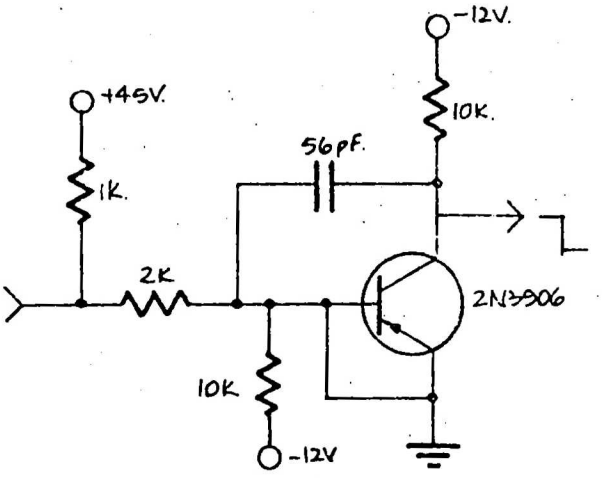


"NEGATIVE IN"

Output Circuits



"POSITIVE OUT"



"NEGATIVE OUT"

The output circuits of this interface are not suited to the "wire-or" connection because of current sinking/sourcing limitations.

A.4.4 Line Driving and the 16-Bit Duplex Register

The manufacture recommends input drive and output receive circuits identical with the output and input circuits on the interface itself.

The transition times of the output circuits would be much greater than those for TTL circuits, because of the capacitor connected between collector and base - rule of thumb estimation indicates a rise time well in excess of 100 nanoseconds. The extreme mismatch between output, line, and input circuits would give rise to a large number of pulse reflections, but, because of the slow rise time, reflections could not occur in cables shorter than about 50 metres. The major drawback, with a line of any length, would be the degradation of rise time caused by the combination of cable capacitance and relatively high source and load resistances. Noise pick-up could be a problem with long rise times and high resistance circuits.

Therefore, this interface should not be used to drive lines if fast response is required. Other applications demanding more than a few metres of line, should be approached with caution and checked for noise immunity.

A.5 Data Source Interface Type 12604B

A.5.1 Application

This interface provides for up to 32 bits to be transferred into the computer; it does not have any data output provision. There is no input storage register; the data must remain on the input lines until transfer is complete.

The primary purpose of this interface is to accommodate output from various Hewlett-Packard test instruments, such as digital voltmeters and counters. Other uses are possible, one in particular being data transfer from real-time clocks, in which nine BCD digits (ddd; hh, mm, ss) are packed into a 32 bit code.

Because signals from such a variety of sources can have wide voltage variations, capacitive coupling is used and a reference voltage must be supplied by the source instrument.

Interrupt circuiting is similar to that previously described (Se. A.1), but the operation and nomenclature of the source/interface control signals is slightly different; the signal usually termed the "flag" signal (indicating that the data is ready) is termed the "record" signal; the device "command" signal is termed the "encode" or "hold" signal, depending on the position of a switch on the interface card. Test instruments take a reading on application of an encode signal (or removal of a hold signal), and, when the reading is complete, issue a record signal to the interface.

Optional interface connections provide for positive - or negative-going record, encode, and hold signals.

This interface is not suitable for fast data transfer; the response time of the data source instruments is normally the limiting factor. A jumper option on the interface board can be set for either 0.1 or 1.0 millisecond delay to allow the data to settle or the input lines after the record signal is received. The 32 data bits are transferred to the computer in two successive timing cycles; the least significant 16 bits being transferred first.

A.5.2 Factory Variations

Options 001 to 006 differ only in the type of inter-connecting cable supplied; the different cables being specific to various test instruments - for details see the operating manual.

Option 020 supplies additional software to enable the interface to be used in the HP 2005 Real Time Executive System.

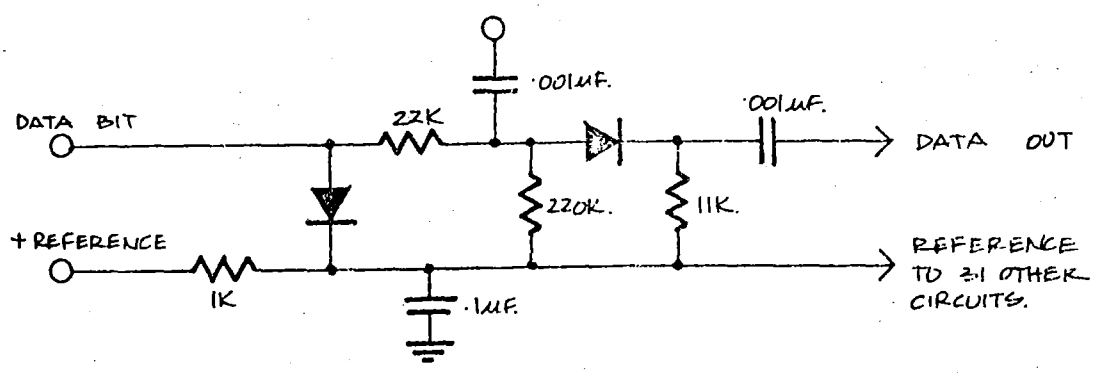
A.5.3 Specifications of Data and Control Signals

Data input "1"	: at least 5 volts positive with respect to data input "0"
Separation, "1" to "0"	: 100 volts maximum
Absolute data levels	: between +100 volts and -100 volts
Input data reference (positive)	: 0.5 volt negative with respect to "1" level. Reference source resistance (maximum) is a function

of the difference between the reference level and "O" level. 4 K ohms (max.) is acceptable for all levels but see curve in manual.

Input data reference (negative)	: Not required by interface, but can be used in cable for setting unused bits to "O" (otherwise may be interpreted as "1"). At least 4.5 volts negative with respect to + Reference and within data levels.
+ Record command	: Positive-going pulse, ac coupled, 4.5 to 24 volts amplitude, 20 microseconds (minimum) duration.
- Record command	: As for + Record, but negative-going.
+ Encode output	: Low: -12 volts through 10 k; High: 0 volts though saturated transistor
- Encode output	: Low: 0 volts though saturated transistor High: +13.5 volts through 9 k.
Pulsed encode	: As above with duration 70 ± 10 microseconds. This function is jumper selected.
+ Hold output	: Low: -12 volts through 100 k; High: +17 volts through 1 k (10 mA max.)
- Hold output	: Low: -11 volts through 2.2 k (10 mA max.) High: +17 volts through 100 k

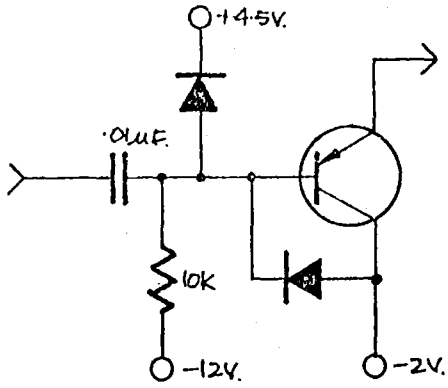
Data Input Circuit



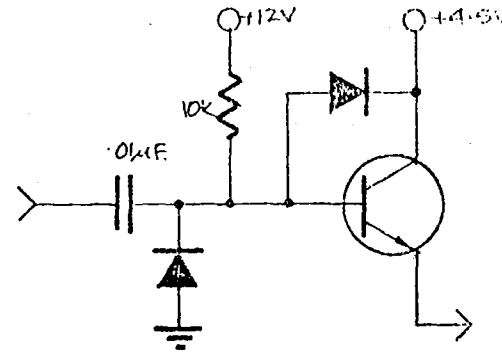
Input high data current: approx. 2 microamps

Input low data current: (+ Reference level - "O" level)/243 k ohms.

Record Input Circuits



+ RECORD



-RECORD

A.5.4 Line Driving and the Data Source Interface

Line driving considerations do not normally arise for applications appropriate to this interface. Speed is unimportant; large logic swings take care of most noise problems; and input impedances are high enough to be regarded as open circuits, thus permitting reverse termination to be used at the source instrument if desired.

Note that the data input levels preclude the use of TTL data sources.

A.6 Digital Input Card, Model 69431A

A.6.1 Application

This interface is intended for use with the H-P 6940A Multi-programmer (and 6941A Multiprogrammer Extender) - a bidirectional 12-bit digital multiplexer. The interface cards associated with the multiprogrammer are designed either for data input or output, not both.

Input data will be stored on the trailing edge of the flag signal from the I/O device. Data must remain on the input lines for at least 3 microseconds after this time. A jumper on the card may be removed to disable the storage register if desired.

The device command signal is termed the gate signal and various options exist for the gate signal timing relative to the flag signal; see the operating manual for details.

As well as data, interrupt, and control circuits, there is a 4-bit address decoder used for card selection in the multiplexing system. The 4 address bits plus the 12 data bits form the 16-bit word processed by the computer.

A.6.2 Factory Variations

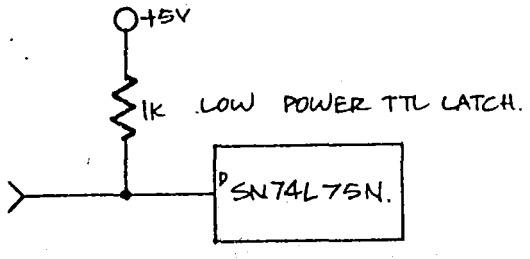
Option 069	:	For inputs having negative-true logic, 0 to +5 volt levels
Option 070	:	For inputs having negative-true logic derived from open collector drives, or relay closures, with levels up to +14 volts
Option 073	:	For inputs having positive-true logic, 0 to +5 volt levels

A.6.3 Specifications of Data and Control Circuits

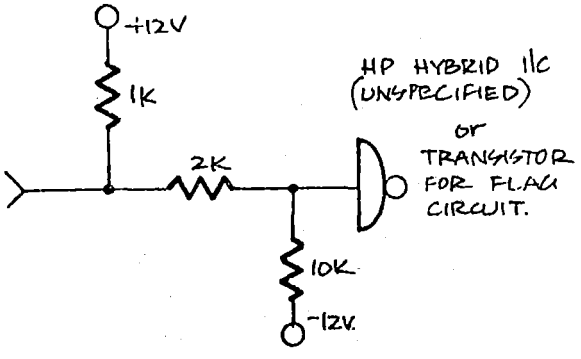
Data input (see note below)	: Options 069 and 073	:	Low: 0 to 0.8 volt (6 mA max); High: +2 to +5 volts
	Options 070	:	Low: 0 to +1 volt (15 mA max); High: +6 to +14 volts
Flag input	: All options	:	Levels as for data inputs; High to low transition indicates device busy; Low to high transition indicates data ready; See note below. Minimum flag duration: 2 microseconds: Minimum transition times: 0.1 volt/ microsecond. Flag input may be left open or connected to gate output.
Gate output (see note below)	: All options		Low: approx. 0 volt from saturated transistor, 11 mA max. sink current; High: +15 volts through 1 k; High to low transition indicates data requested; Low to high transition normally triggered by leading edge of flag signal but user can select trailing edge.

Note: The specifications given above refer to the card as supplied by the manufacturer. By means of circuit board jumpers and the addition of input bias components, the board can be modified to accept a wide range of input levels, to invert logic for one or more bits, and to invert the logic for the flag and/or gate signals.

Input Circuits

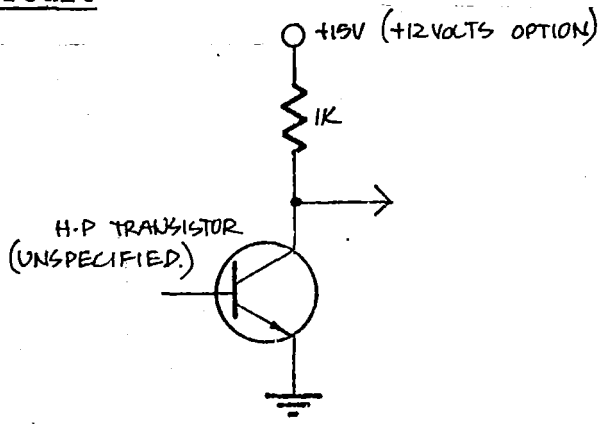


Options 069, 073



Option 070 and Flag

Gate Output Circuit



A.6.4 Line Driving and the Digital Input Card

Driving the data input lines to this interface differs very little from driving those to the Microcircuit Interface; the slightly higher input resistance will increase the number of pulse reflections, but the Bergeron diagram gives waveforms virtually the same as those in figure A.2 for options 069 and 073. Option 070 and the flag input cannot be driven from TTL circuits because of differing voltage levels. Line driving effects for these inputs and the gate output should be checked for each I/O device application.

For options 069 and 073 the remarks in Section A.3.4 regarding reverse termination, are applicable.

A.7 Other Interfaces

Hewlett-Packard manufacture many other interfaces and a few of the less specialised ones will be mentioned briefly.

A.7.1 Time Base Generator 12539C

This provides time intervals, from 100 microseconds to 1000 seconds, for internal computer use only. It is not strictly an interface, but can eliminate the need for an external timer.

A.7.2 Relay Output Register 12551B

This has a 16-bit output register, providing contact closures to the external device.

A.7.3 Digital to Analogue Converter 12555B

Two independent 8-bit registers each have analogue outputs of 0 to +10 volts. It is worth noting that an 8 channel, 10-bit/channel, interface card has been designed in the BMR laboratory by A.B. Devenish, and will be used in the marine system. The BMR unit can handle positive and negative numbers, with an output range of -5 volts to +5 volts.

A.7.4 Universal Interface 12930A

This is a 16-bit input/output interface with differential drivers for high speed extended distance transmission.

A.7.5 Buffered Teleprinter Interface 12531C and High Speed Terminal Interface 12531D

As the names imply, these are intended for use with teleprinters, thermal printers, visual display units, etc. An internal crystal oscillator and divider chain sets the bit rate appropriate to the I/O device. The two units are basically the same, but have different oscillator frequencies and voltage levels to accommodate a range of industry standards. Operation from an oscillator in the I/O device is possible.

Application of these units could be extended to any I/O device having an 8-bit serial data format.

A.7.6 Interface Breadboard 12620A

This is a card containing standard control and interrupt circuits only. The 49 blank integrated circuit receptacles remaining may be used for implementing special interface requirements designed by the user.

SOURCE INSTRUMENTS.

I.R.I.G. E SERIAL TIME CODE

1 ANALOGUE CHANNEL

SLOW CODE TO TIME MARK UNIT.

DIGITAL

DIGITAL SENDING INTERFACES.
6 MODULES / BIN
13 BITS / MODULE.

TRANSMISSION LINES.
1 TWISTED PAIR / BIT.

DIGITAL RECEIVING INTERFACES.
10 MODULES / BIN
12 BITS / MODULE

TRANSMISSION LINES.

SENDER No.1 (4 MODULES)

CLOCK No.1 — ddd., hh., mm., ss., DAYS, HRS, MIN., SEC. 1 HZ, 10 HZ
9 BCD DIGITS (ENCODED) BUSY BIT
2 BINARY BITS.
MAINS
8 BITS, 12 BITS, 12 BITS, 12 BITS, P/S

CLOCK No.2 — DAYS, HRS., MIN., SEC.
9 BCD DIGITS (ENCODED) BUSY BIT
MAINS
8 BITS, 12 BITS, 12 BITS, 12 BITS — SENDER No.2 (3 MODULES)

MAGNETIC GRADIOMETER SENSOR No.1 / SENSOR No.2
6 BCD DIGITS, BUSY BIT — 12 BITS, 12 BITS
6 BCD DIGITS, BUSY BIT — 12 BITS, 12 BITS
MAINS
12 BITS, 12 BITS, 12 BITS, 12 BITS — SENDER No.3 (4 MODULES)

GRAVIMETER — SPRING TENSION, COMPUTED GRAVITY.
6 BCD DIGITS, BUSY BIT — 12 BITS, 12 BITS
6 BCD DIGITS, BUSY BIT — 12 BITS, 12 BITS
MAINS
12 BITS, 12 BITS, 12 BITS, 12 BITS — SENDER No.4 (4 MODULES)
S/D CONVERTERS MAY BE REQUIRED.

FATHOMETER No.1 (RAYTHEON?)
5 BCD DIGITS, 6 BINARY STATUS BITS, BUSY BIT
MAINS.
8 BITS, 12 BITS, 6 BITS, 12 BITS — SENDER No.5 (3 MODULES)

DEPTH SOUNDER — BACK-UP TYPE TO BE DECIDED.
5 BCD DIGITS, 6 BINARY STATUS BITS, BUSY BIT
MAINS.
8 BITS, 12 BITS, 6 BITS, 12 BITS — SENDER No.6 (3 MODULES)

GYRO COMPASS No.1 — MAY REQUIRE S/D CONVERTER.
VELOCITY LOG X, Y.
4 BCD DIGITS, BUSY BIT
3 BCD DIGITS, BUSY BIT
3 BCD DIGITS, BUSY BIT
MAINS
4 BITS, 12 BITS, 12 BITS, 12 BITS, 12 BITS — SENDER No.7 (4 MODULES)

DOPPLER ECHO COUNTS
5 BCD DIGITS, BUSY BIT
MAINS
12 BITS, 12 BITS, 12 BITS, 12 BITS — SENDER No.8 (4 MODULES)

WATER VELOCITY
5 BCD DIGITS, BUSY BIT
MAINS.
8 BITS, 12 BITS, 4 BITS, 12 BITS — SENDER No.9 (4 MODULES)

PROCESSED TATAL DISTANCE
7 BCD DIGITS, 8 BCD DIGITS, BUSY BIT
MAINS
12 BITS, 8 BITS, 12 BITS, 12 BITS, 12 BITS — SENDER No.10. (4 MODULES)

DEPTH TO REFLECTOR.
5 BCD DIGITS, BUSY BITS.
MAINS
8 BITS, 12 BITS — SENDER No.11. (2 MODULES)

GYRO COMPASS No.2 (BACK UP) — MAY REQUIRE S/D CONVERTER.
4 BCD DIGITS, BUSY BITS.
MAINS.
4 BITS, 12 BITS — SENDER No.12 (2 MODULES)

NOTE: THIS DISTANCE TO BE AS SHORT AS POSSIBLE PREFERABLY < 1 METRE.

66 DATA BITS. 2 BUSY BITS. 1 PWSB/GGC. TO TIME MARK UNIT.
RECEIVER No.1 (7 MODULES) — LATCHED OUTPUT. UNLATCHED OUTPUT. 10 P.P.S., 1 P.P.S., MAINS.
2 ENCODE BITS, 2 RECORD BITS. — 2 REFERENCE LINES (HIGH LEVEL FROM RECEIVER No.1 ONLY TO DRIVE 32 BIT INTERFACE.)

56 DATA BITS. 4 BUSY BITS.
RECEIVER No.2 (8 MODULES) — 8 GATE BITS, 8 FLAG BITS.
12 BCD DIGITS (4 DAC CHANNELS) U — MAINS

52 DATA BITS. 2 BUSY BITS.
RECEIVER No.3 (6 MODULES) — 8 GATE BITS, 8 FLAG BITS.
6 BCD DIGITS (2 DAC CHANNELS) U — MAINS

92 DATA BITS. 3 BUSY BITS.
RECEIVER No.4 (8 MODULES) — 8 GATE BITS, 8 FLAG BITS.
9 BCD DIGITS (3 DAC CHANNELS) GYRO VELOCITY. U — MAINS

80 DATA BITS. 2 BUSY BITS.
RECEIVER No.5 (8 MODULES) — 8 GATE BITS. 8 FLAG BITS.
6 BCD DIGITS (2 DAC CHANNELS) P.D.T. U — MAINS

40 DATA BITS. 2 BUSY BITS.
RECEIVER No.6 (4 MODULES) — 4 GATE BITS. 4 FLAG BITS.
3 BCD DIGITS (1 DAC CHANNEL) GYRO. U — MAINS

12 DAC CHANNELS.
16 CHANNEL DAC — MAINS
8 MODULES / BIN. 2 CHANNELS / MODULE. 12 BITS (= 3 BCD DIGITS) / CHANNEL.
12 ANALOGUE CHANNELS. 1 SHIELDED TWISTED PAIR / CHANNEL.

AMP / FILTER BIN No.1 (6 MODULES) — MAINS
AMP / FILTER BIN No.2 (6 MODULES) — MAINS
8 MODULES / BIN. 1 CHANNEL / MODULE.

6 CHANNELS
6 CHANNELS

L.S.B. PROCESSED TOTAL DISTANCE.
TIME (CLOCK 1)
TIME (CLOCK 2)
1 BIT 1 PPS

V.D.U. TEKTRONICS 4010 — 10.

SEISMIC SYSTEM.

SHOT TIMING & RECORDER TIMING UNIT.

CPU — CPU COMMUNICATION.

H.P. 7905 DISC. CPU — CPU COMMUNICATION.

SEISMIC 32K C.P.U.

CPU No.1 32K
22 BIT — 32 BIT
16 BIT MICRO CIRCUIT. 16 BIT DUPLEX.
P.T.R. TTY
CPU — CPU COMMUNICATION
SHOT INTERVAL
TAPE CONTROL — 3 BCD DIGITS
DISTANCE CONTROL — 1 BINARY BIT
16 BIT REGISTER.
(DMA) MAG. TAPE CONTROLLER.
(DMA) CPU — CPU COMMUNICATION.
16 BIT MICROCIRCUIT.
8 CH. DAC
8 CH. DAC
8 CH. DAC

MULTI PROGRAMMER. 15 INPUT CARDS. (12 BITS / CARD) No.1
EXTENDER 1. 15 INPUT CARDS.
EXTENDER 2. 15 INPUT CARDS.

PAPER TAPE READER.

TELEPRINTER No.1 (N.C.R.)

SATELLITE DOPPLER — NAV. COMP.

CPU — CPU COMMUNICATION.
CPU No.2 32K
TTY
16 BIT MICRO-CIRCUITRY.
PTR
PTP
X.Y. PLOTTER.

X-Y PLOTTER

DIGITAL MAG. TAPE No.1 (9 TRACK)
DIGITAL MAG. TAPE No.2. (9 TRACK)
TELEPRINTER No.3 (N.C.R.)
H.P. 9871 IMPACT PRINTER.
PAPER TAPE READER.
PAPER TAPE PUNCH

A/D CONVERTER. 18 CHANNELS. (PHOENIX.)
40 CHANNELS
32 ANALOGUE CHANNELS. 1 SHIELDED TWISTED PAIR PER CHANNEL.

PATCH PANEL

19 ANALOGUE CHANNELS

1 PULSE PER 10 MIN
SLOW CODE FROM CLOCK
TIME MARK UNIT
10 MIN MARK
SLOW CODE
5 CHART RECORDERS 4 OR 6 CHANNELS

SOURCE INSTRUMENTS.

AMPLIFIERS / FILTERS
1 MODULE / CHANNEL
2 IDENTICAL OUTPUTS / MODULE
8 MODULES / BIN

ANALOGUE

1 SHIELDED TWISTED PAIR PER ANALOGUE CHANNEL.

AMP./FILTER BIN No.3 (8 MODULES) — MAINS.
3 CHANNELS B, Hx, Hy.
1 CHANNEL
2 CHANNELS

AMP./FILTER BIN No.4 (8 MODULES) — MAINS
8 CHANNELS.
18 CHANNELS.

GRAVIMETER.
BEAM POSITION
HORIZONTAL ACCELERATION
INTERMEDIATE CHANNELS.

NAVIGATION SYSTEMS.
GYRO COMPASS No.1
TORQUE CORRECTION
PITCH & ROLL
SONAR DOPPLER.

AMP./FILTER BIN No.5 (8 MODULES) — MAINS
1 CHANNEL
2 CHANNELS

V.L.F.

AMP./FILTER BIN No.6 (8 MODULES) — MAINS
8 CHANNELS
6 CHANNELS
AMPLITUDE.

AMP./FILTER BIN No.7 (8 MODULES) — MAINS
8 CHANNELS
6 CHANNELS
PHASE.

AMP./FILTER BIN No.8 (8 MODULES) — MAINS
UP TO 4 CHANNELS

ATMOSPHERIC SYSTEMS.
3 CHANNELS — WIND VELOCITY.
1 CHANNEL — AIR PRESSURE.
1 CHANNEL — TEMPERATURE.
1 CHANNEL — HUMIDITY.

AMP./FILTER BIN No.9 (8 MODULES) — MAINS
UP TO 2 CHANNELS.

OCEANOGRAPHIC SYSTEMS.
1 CHANNEL — WATER TEMPERATURE.
1 CHANNEL — SALINITY.

NOTE:- DISTANCE BETWEEN SOURCE AND AMPLIFIERS TO BE AS SMALL AS POSSIBLE.

LEGEND.
ITEM TO BE PURCHASED.
* ITEM TO BE BUILT.
ALL OTHER ITEMS AVAILABLE.

NOTE: MAINS SUPPLIES SHOWN ONLY FOR ITEMS TO BE BUILT.

REVISED 4-2-76, 17-3-76 - FSC., 26-7-76 - P.B.

BUREAU OF MINERAL RESOURCES GEOLOGY AND GEOPHYSICS 203 COLLINS STREET, MELBOURNE, VICTORIA GEOPHYSICAL LABORATORIES, FOOTSCRAY	MATERIAL / SCALE	DATE 12-1-76 / NAME R. Lam.	1977 MARINE DATA ACQUISITION SYSTEM.	BLOCK DIAGRAM.	DRAWING No. ZXD_1 SHEET 1