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1979/66

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Geology and Geophysics

Development of 8-channel digital-to-analogue conversion card for HP 2100 series computers

by

A.B. Devenish

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1. Introduction

Hewlett Packard manufactures a two-channel digital-to-analogue conversion card for use in HP 2100 series computers. In BMR applications, however, the airborne system requires the monitoring of 7 quantities, the magnetotelluric system 5, and the marine system 4. For this reason, it was decided to develop an 8-channel digital-to-analogue (D/A) conversion card for use in HP 2100 computers.

An HP 12620A breadboard card was available for trying test circuits. First one channel was constructed and tested using CMOS logic; this logic type was found to be too slow to be used. Next a test circuit was constructed using TTL logic; this proved satisfactory. Low-power TTL was used in the production cards to reduce the amount of power used and heat produced. This was necessary since the final card contains 50 integrated circuits.

Three types of D/A chips made by Precision Monolithics Inc. were tested. They were the DAC 100, DAC 02, and DAC 04. The DAC 100 is a straight binary input, 0-10 volt output device. The DAC 02 is a sign magnitude input device with a -10 to +10 volt output. The DAC 04 is a 2's complement input device with a -5 to +5 volt output. One complete card was made using DAC 100 chips. This card worked correctly. However, BMR's marine group decided that they preferred a card using 2's complement D/A converters. Ten cards were made using 2's complement D/A converters.

2. Functional Description

The function of this card is to receive 13 data bits and 21 signal lines from the back plane of a HP 2100 computer. Three bits are used to determine which of the analogue outputs is selected. The other 10 bits contain the data to be converted to an analogue voltage. The data bits are in 2's complement form.

The flag, interrupt and control circuitry on the board is used for the control of interrupts. When the control flip-flop is set, the computer is ready to receive an interrupt and, when the flag flip-flop is set, an external device has requested an interrupt. This part of the circuitry was added to so it could function in three ways:

(i) An external device can set the computer flag.

(ii) The flag can be set at preset time after being cleared.

(iii) Setting the flag causes the program to jump to the memory location equal to the select code of the card.

Choice of operating mode is determined by hand-wired links.

3. Circuit Description

Block Diagram

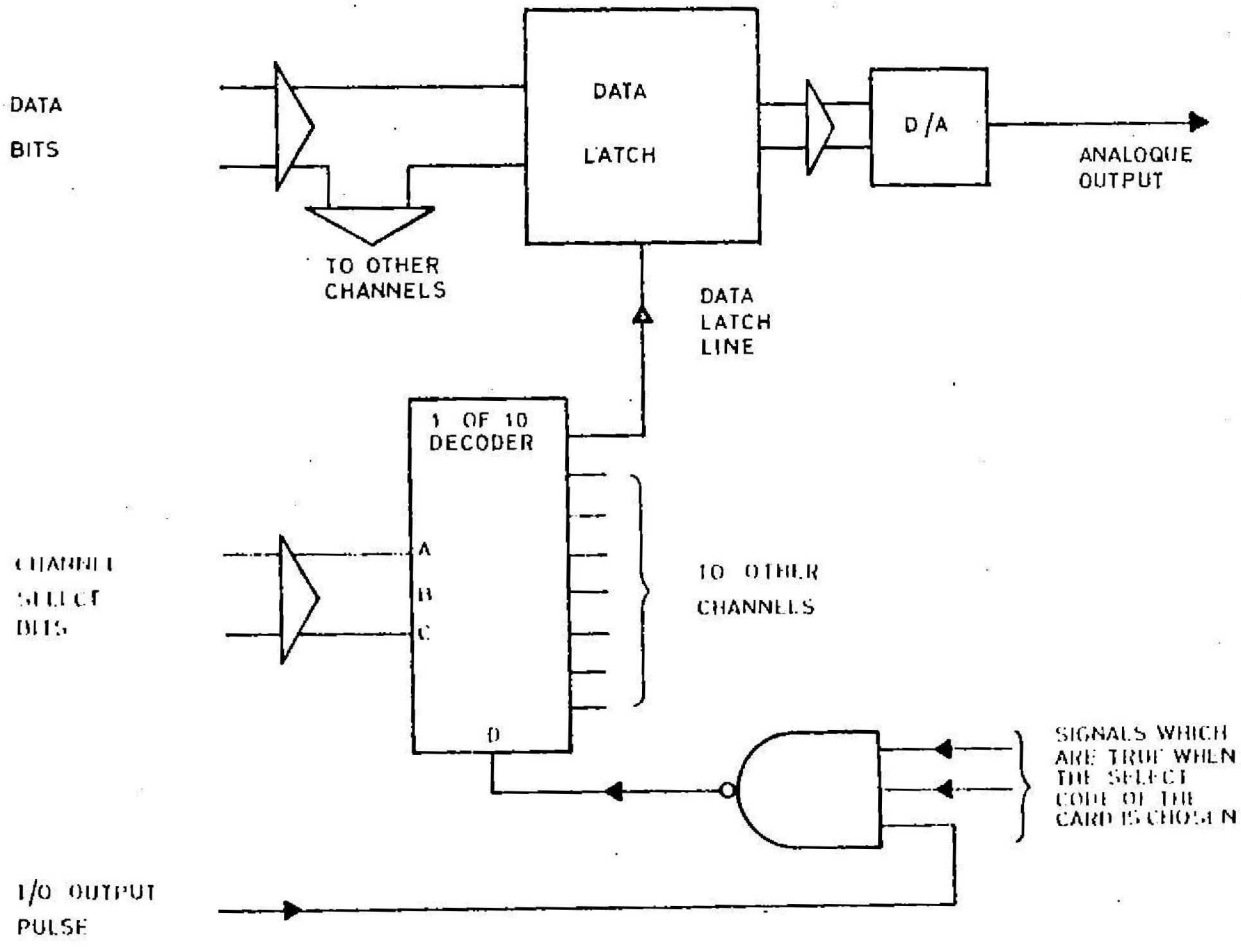


Fig. 3.1

The card receives 13 bits from the computer. Three of these are used to determine which of the eight D/A channels is to receive the ten data bits. This is achieved using a 1 of 10 decoder type 9301. The A, B and C inputs are used to determine which output line goes low and enables the data of a certain channel. The D latch input is used to disable the selection of one of the eight channels when it is not required. The truth table for the 9301 decoder is as follows:

Inputs				Outputs									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

9301 Truth Table

Fig. 3.2

It can be seen from the truth table that when D is high none of the channels 0 to 7 can be low. Input D only goes low when the select code of the card is chosen and a OTA/B* instruction is given e.g. OTA 11 when the card is in slot 11. This enables the card to ignore all the data on the lines except when an OTA/B* instruction to the card's select code is executed.

When the data latch line is low, the output of the data latch follows the input. When it goes high, the output is latched. The data and latch pulse time relationship is represented in the following diagram.

Latch Pulse and Data Pulse time relationship

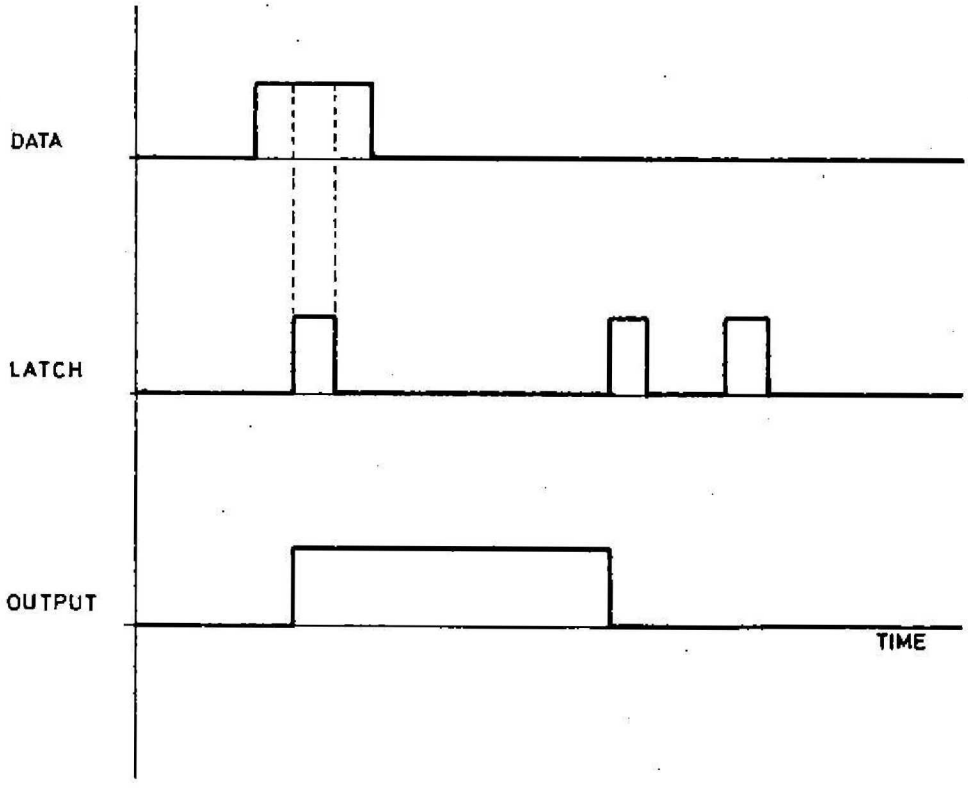


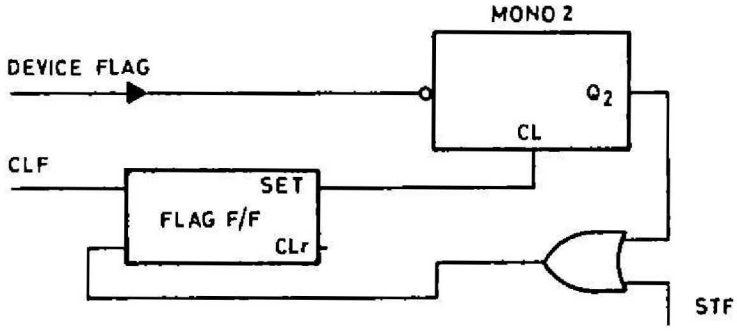
Fig. 3.3

*OTA/B - output the A or B register

The flag and interrupt circuitry is a copy of the standard Hewlett Packard flag and interrupt circuitry found on the Hewlett Packard breadboard card type 1260. A few extra components were added to enable the computer program to loop for an adjustable period. This was to allow time for pen movement if the card was used to drive a chart recorder. The magnetotelluric system required that the flag flip-flop could be set from an external device. Provision was made for this mode of operation.

A summary of the three ways the flag and interrupt circuitry can be used are as follows:

(a) An external device can set the flag on the card.



Device flag interrupt Fig. 3.4

An external device triggers mono 2 which toggles the flag flip-flop. When set goes high, it clears mono 2. To be operated this way, the output from mono 1 is disconnected from mono 2 and the input of mono 2 is connected to the device flag.

(Links d - f and a - c connected)

(b) The flag is set at preset time after being cleared.

Time delay interrupt

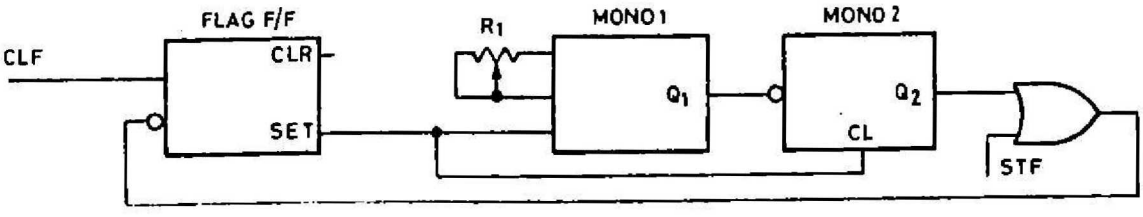


Fig. 3.5

The clear flag instruction (CLF) causes the set output of the flag flip-flop to go low. This triggers monostable 1 which causes Q1 to go high for a time adjustable by R1. When Q1 goes low again monostable 2 is triggered which causes Q2 to go high. This in turn toggles the flag flip-flop which causes the set side to go high again which clears monostable 2.

(Links e - f and c - a connected).

(c) If the user doesn't wish to use either of the first two options, he can disable both of them by disconnecting the monostable from the flag flip-flop.

(Link a - b connected)

Normal interrupt

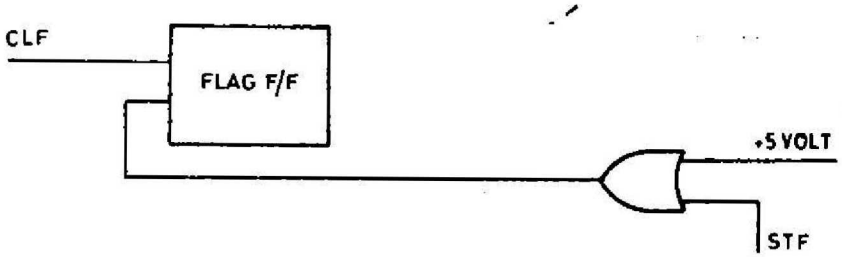


Fig. 3.6

4. Specifications

1. Physical Dimensions 196.8 mm x 220.7 mm

   (Designed to fit into a HP 2100 computer mainframe).

2. Word format

   Bits 0-2 for channel selection

   Bits 15-6 for data input

3. Logic format

   The DAC chips used are 2's complement devices. The following table shows output for given inputs.

DAC 04 Input/Output Table

Input										Output
0	1	1	1	1	1	1	1	1	1	5.000volt
0	1	1	1	1	1	1	1	1	0	4.990 volt
0	0	0	0	0	0	0	0	0	1	0.010 volt
0	0	0	0	0	0	0	0	0	0	0.000 volt
1	1	1	1	1	1	1	1	1	1	-0.010 volt
1	0	0	0	0	0	0	0	1	0	-4.990 volt
1	0	0	0	0	0	0	0	0	1	-5.000 volt

4. Logic Type.

TTL and low power TTL

5. Interrupt, flag and control circuitry.

The board contains the logic circuitry of the HP 12620A breadboard card plus extra components to carry out the following functions:

(i) Set the flag at preset time after being cleared.

(ii) Set the flag from an external device.

5. Testing

Various programs have been written to test the cards. The simplest being to output data from the switch register to the card. The code for it is as follows:

```
START    LIA 1        Load the A register from the
                      switch register

         OTA SC       Output the A register to the card

         JMP          START    Jump back to start.
```

This program enables the checking of DC voltages out for various data inputs for each channel.

Another program which outputs DC ramps for each channel is as follows:

```
         LDA  X  )    Increment the A register by 100(8) to
START    ADA  X  )    increment the analogue output.

         CCB     )    Use the B register as channel
LOOP     INB     )    select.

         CPB  Y       Check for last channel

         JMP  START ) If last channel increment A
                    ) register by 100(8).

         IOR  1       Form word with data and channel select
         OTA  SC      Output word to card.

         AND  MASK    remove the channel select from the card.

         JMP  LOOP
```

MASK 177700_8

Y 10_8

X 100_8

Part of the airborne software package includes a test of the 8 channel D/A card using a chart recorder.

Programs to test the three modes of operation of the flag and interrupt circuitry are as follows:

(a) The flag is set a preset time after being cleared. (e - f and c - a connected).

```
START   CLF     SC          clear flag
        SFS     SC      )   wait for flag to be set
        JMP     * - 1   )
        INA                 Increment A
        OTA 1               Output A to the switch register
        JMP     START
```

Changing the monostable timing resistor changes times between counts as seen on the switch register.

(b) The flag is set by an external device. (d - f and c - a connected).

```
START   CLF     SC          clear flag
        SFS     SC      )   wait for flag to be set
        JMP     * - 1   )
        INA                 Increment A
        OTA     1           Output A to the switch register
        JMP     START
```

Each time an external device flag is received, the A register and switch register imcrement.

11

(c) An internal interrupt causes the program to jump to the memory location of the cards select code. (a - b connected).

```
START       STF,  0       enable interrupt system
            STF   SC      interrupt

SC          JMP           GO

GO          INA           Increment A
            OTA   1       Output A to the switch register
            JMP   GO
```

The program is started at START and jumps to GO which can be seen by the counting of the switch register.

6. Usage

The cards are used in computers in the airborne survey aircraft, magnetotelluric survey truck, marine data acquisition system and magnetogram digitiser. In the magnetotelluric system, it is used to monitor analogue outputs of the three magnetic channels and two electric channels recorded. In the airborne system, they produce analogue outputs of the four radiometric channels, altitude, magnetometer and Doppler navigation information.

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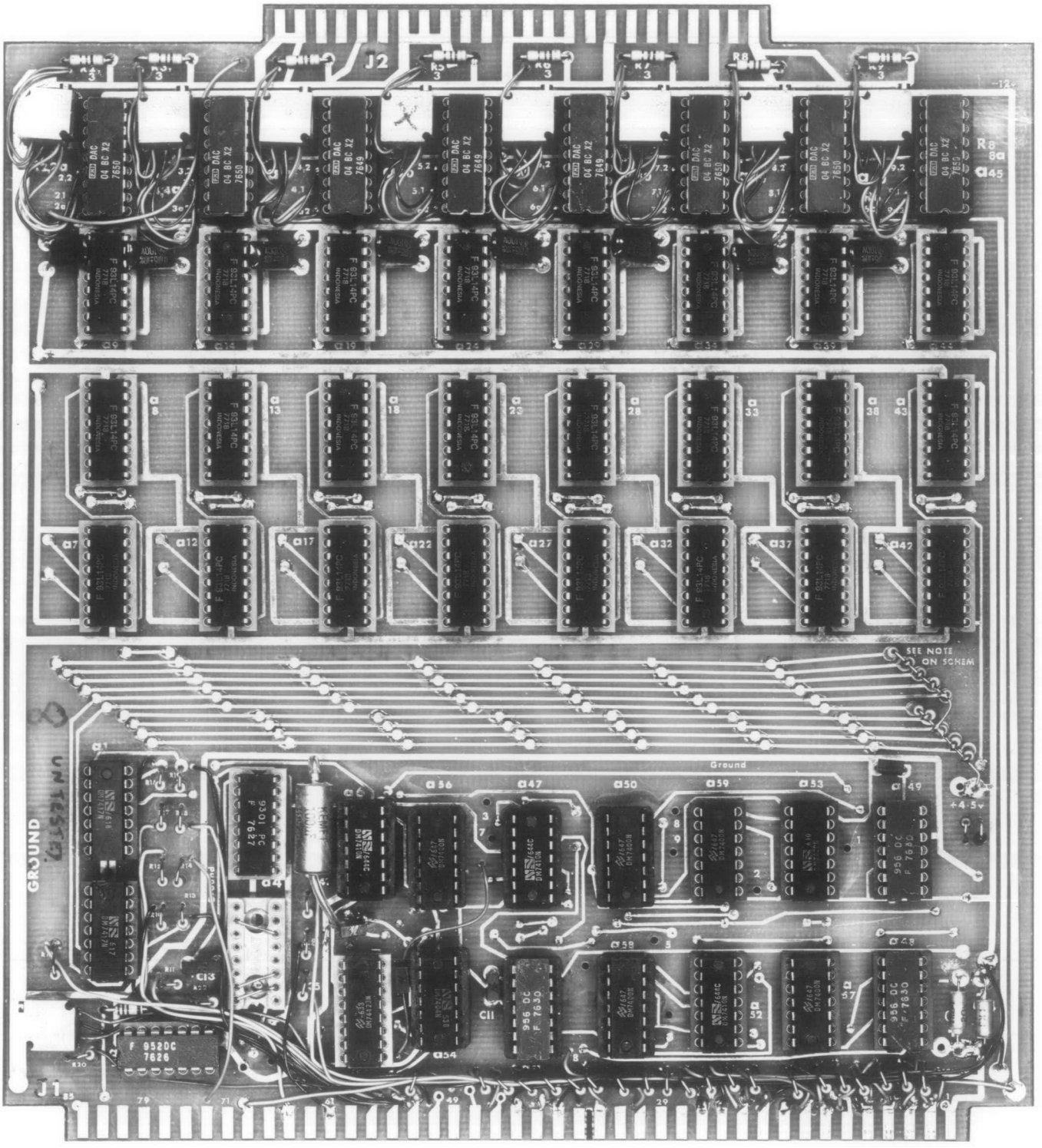

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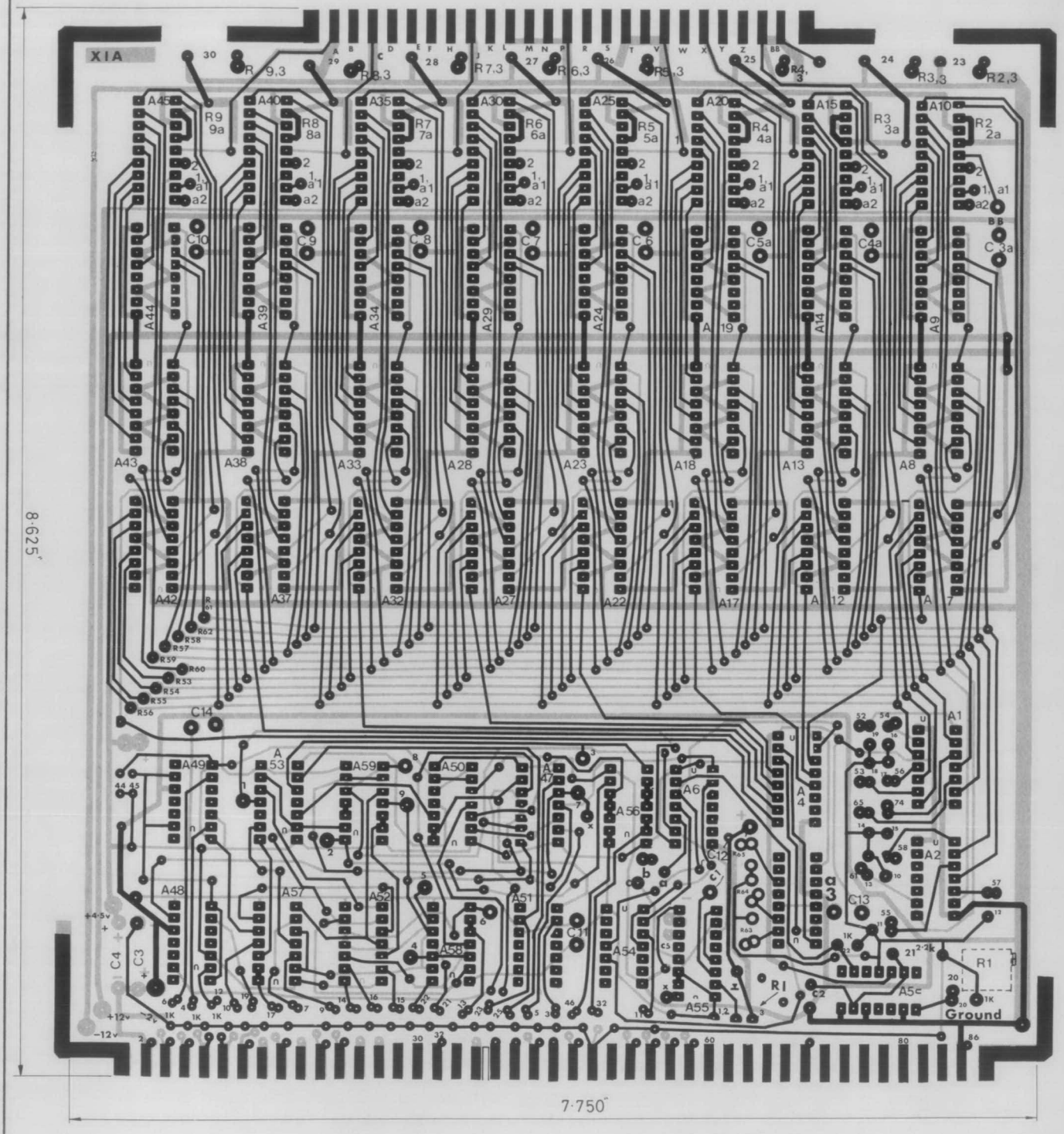
	R. GAN
MODULE	**DATE**
8 CHANNEL D/A CONVERTER.	16-2-76.

DRAWING No.	SHEET
	1 (v). 13



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INSTRUMENT	DRAWN
	R. GAN

MODULE	DATE	DRAWING No.	SHEET
XIA-1 8 CHANNEL D/A CONVERTER.	16-2-76	X7	1 (iv). 14

PARTS LIST

ITEM	VALUE	W.v.	Tol. %	TYPE	MAKE	MAKERS REF.	BMR VOCAB	QTY
A1, 2.				HEX. BUFFERS/DRIVERS	TEXAS INST.	SN7417N	BUT-7417N	2.
A4.				4 INPUT. 1 OF 10 DECODER	FAIRCHILD	9301	BUS_6B9301	1.
A5.				DUAL 2-INPUT NOR GATE	"	9952PC	BUE_992PC	1.
A6, 47, 52.				TRIPLE 3-INPUT NAND GATES	TEXAS INST.	SN7410N	N.I.V.	3.
A7, 8, 9, 12, 13, 14, 17, 18, 19, 22, 23, 24, 27, 28, 29, 32, 33, 34, 37, 38, 39, 42, 43, 44.				4 BIT D. LATCHES	FAIRCHILD	93L14PC	BUS_93L14PC	24.
A10, 15, 20, 25, 30, 35, 40, 45.				TWO'S COMPLEMENT 10 BIT D/A CONVERTER	P.M.I.	DAC-04BCX2	BUZ_04BCX2	8.
A48, 49, 51.				DUAL 2-INPUT BUFFER	FAIRCHILD	9956PC	BUE_9956PC	3.
A50, 56, 57, 58, 59.				QUAD 2-INPUT NAND GATES	TEXAS INST.	SN7400N	BUT_7400N	5.
A53.				DUAL 4-INPUT NAND GATES	"	SN7420N	BUT_7420N	1.
A54.				HEX. INVERTERS	"	SN7404N	BUT-7404N	1.
A55.				DUAL RT MONO MULTIVIBRATOR/CLR	"	SN74123N	N.I.V.	1.

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INSTRUMENT:
8 CHANNEL D/A CONVERTER.

COMPONENTS: I.C.'S

SHEET Nº: 46 | ISSUE 1.

MODULE: X1A-1 | DATE 21/8/79. 15

PARTS LIST

ITEM	VALUE	W.v.	Tol. %	TYPE	MAKE	MAKERS REF.	BMR VOCAB	QTY
C6	100uF	10V	20	SOLID TANTALUM CAPACITOR.	KEMET	T110C-107K-0010AS.	BCK_02107	1.
C2.	1200pF	100V	10	CAPACITOR, CERAMIC, CK.	VITRAMON	CK05BX-122K.	BCA_1122	1.
C3, 4.	2·2μF	20 V		CAPACITOR, SOLID TANTALUM.	KEMET	T110A-225K-020AS.	BCK_03225	2.
C3a, 4a, 5a, 6a, 7-11, 14.	0·01μF	100V	10	CAPACITOR. CERAMIC, CK.	VITRAMON	CK05BX-103K	BCA-1103	10.
C13.	1500pF	100V	10	CAPACITOR, CERAMIC, CK.	"	CK05BX-152K	BCA_1152	1.
C5.	1000pF	200	10	CAPACITOR, CERAMIC, CK.	"	CK05BX-102K	BCA_2102	1.
R1.	5KΩ			½W TRIMPOT, 25TURN.	BOURNS	3282L	BPC_3502	1.
R2_9, R2a_9a.	20KΩ			½ TRIMPOT 25 TURN	"	3282L	BPC_3203	16.
R10_19, 32-43, 63-65,	1·5KΩ	0.4W	2	RESISTOR, METAL FILM, MR25.	PHILIPS	2322-151-41502	BRA_55152	25.
R21.	2·2KΩ	"	"	RESISTOR, METAL FILM, MR25.	"	2322-151-42202	BRA-55222	1.
R22, 53a, 46_52, 53_62.	1KΩ	"	"	RESISTOR, METAL FILM, MR25.	"	2322-151-41002.	BRA_55102	19.
R23_30.	62KΩ	"	"	RESISTOR, METAL FILM, MR25.	"	2322-151-46203.	BRA_55623	8.
R44.	360Ω	"	"	RESISTOR, METAL FILM, MR25.	"	2322-151-43601	BRA-55361	1.
R45.	200Ω	"	"	RESISTOR, METAL FILM, MR25.	"	2322-151-42001	BRA_55201	1.

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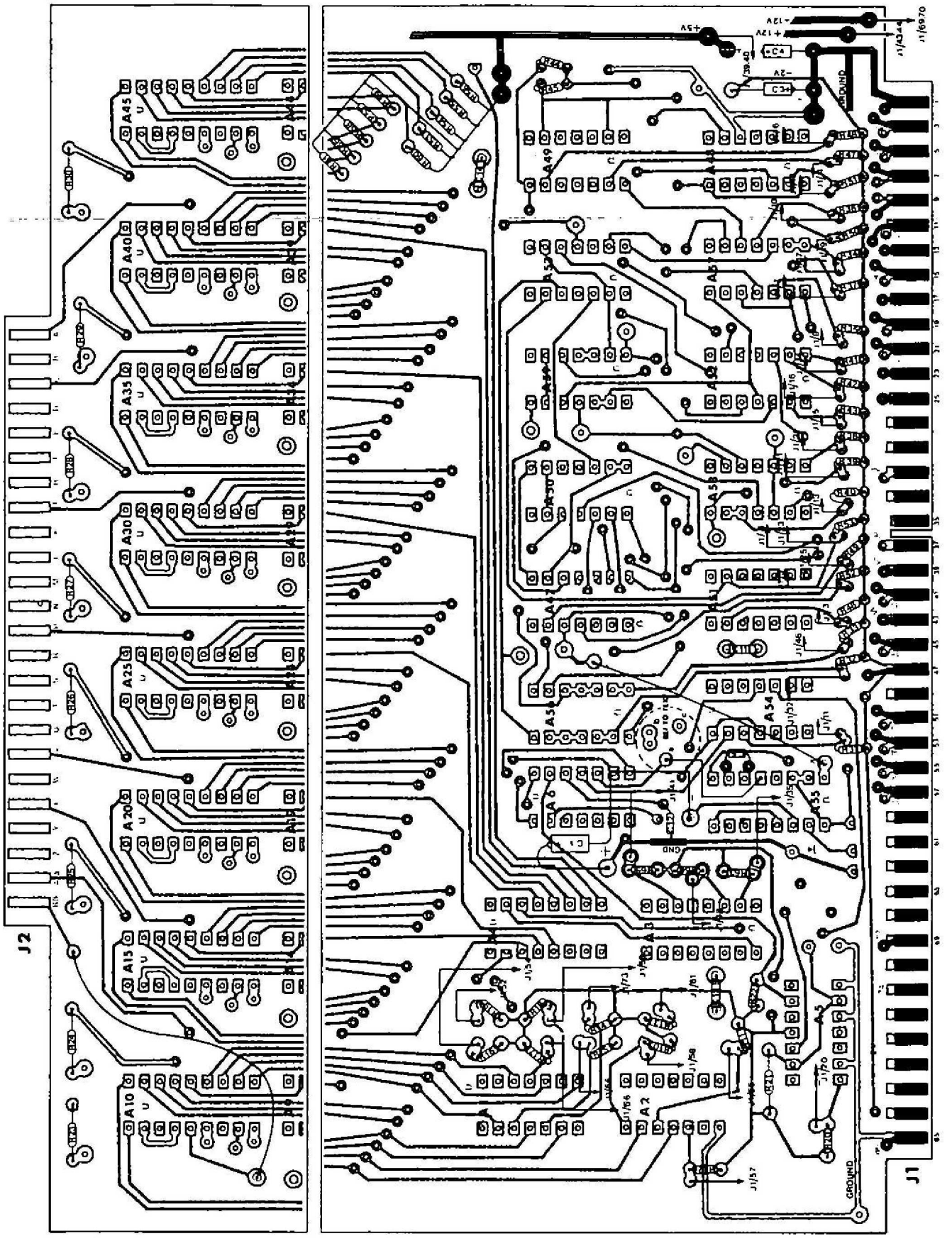
MODULE: XIA-1
DATE 21/8/79.



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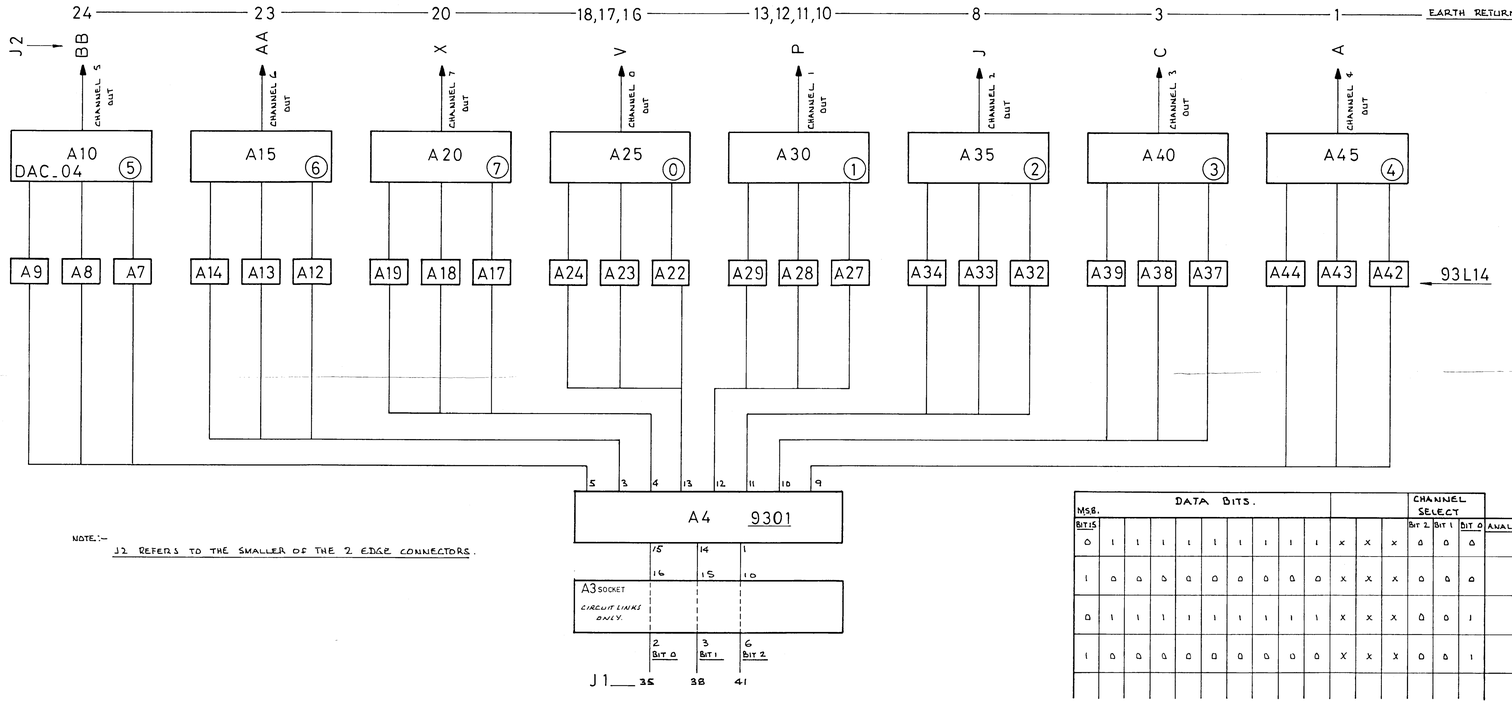
MODULE X1A-1. 8-CHANNEL D/A CONVERTER (Hard-wired Diagram)	k.a.mort	X7	2 17
	DATE 6/9/79		

DRAWN	DATE	C'K'D	AMENDMENTS	ISSUE
R. Lan	17/8/77			1
H.P. Nicol	17.5.79		IC A3 DELETED SOCKET NOW USED AS CIRCUIT LINK.	2



NOTE:- J2 REFERS TO THE SMALLER OF THE 2 EDGE CONNECTORS.

	MSB. DATA BITS.												CHANNEL SELECT					
	BIT 15												BIT 2	BIT 1	BIT 0	ANALOGUE OUT V.	PIN OUT.	
CHANNEL 0	0	1	1	1	1	1	1	1	1	1	X	X	X	0	0	0	+5 VOLTS.	V	CHANNEL 0
	1	0	0	0	0	0	0	0	0	0	X	X	X	0	0	0	-5 VOLTS.	V	
CHANNEL 1	0	1	1	1	1	1	1	1	1	1	X	X	X	0	0	1	+5 VOLTS.	P	CHANNEL 1
	1	0	0	0	0	0	0	0	0	0	X	X	X	0	0	1	-5 VOLTS	P	

BUREAU OF MINERAL RESOURCES, GEOLOGY AND GEOPHYSICS CNR. CONSTITUTION AVENUE & ANZAC PARADE CANBERRA, A.C.T	DRAWING No. X7	SHEET 3	INSTRUMENT 8 CHANNEL D/A CONVERTER BLOCK DIAGRAM SHOWING CHANN. OUT.

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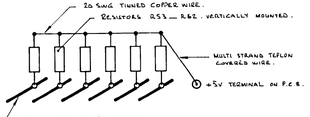
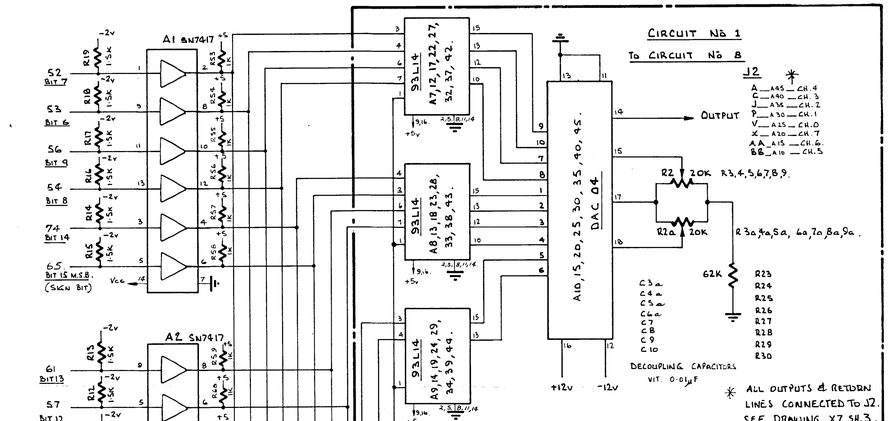
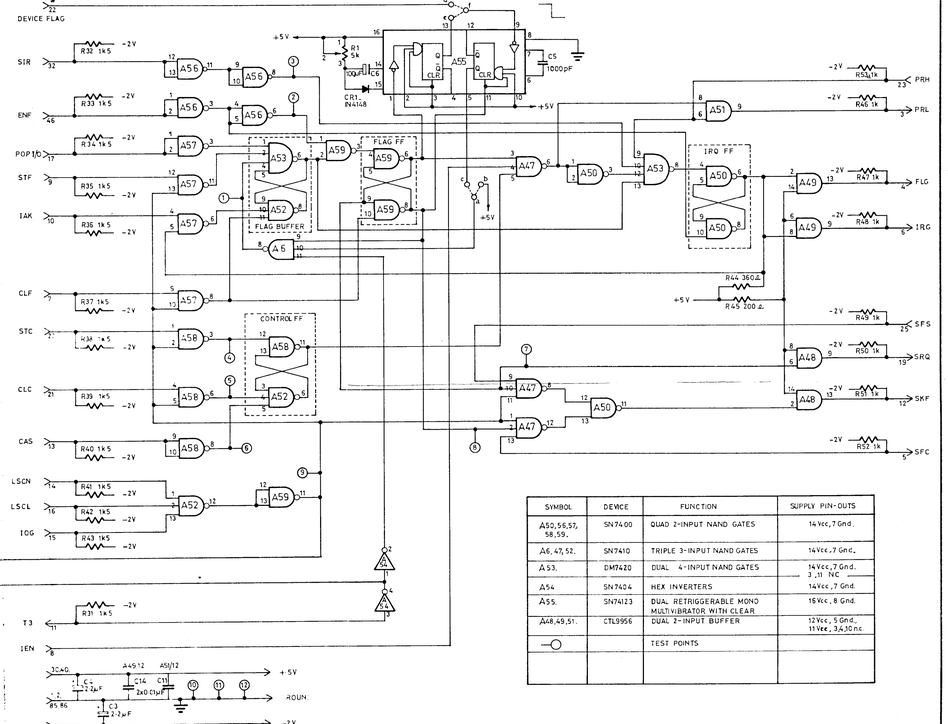
R. GAN	23.3.76		VARIOUS	2
K.A.HART	17/8/77		GATING CIRCUITRY REDRAWN, DELETE A3	3

NOTE:-



MOUNTING PROCEDURE FOR RESISTORS R53-R62.





SYMBOL	DEVICE	FUNCTION	SUPPLY PIN-OUTS
A50,56,57, 58,59.	SN7400	QUAD 2-INPUT NAND GATES	14 Vcc, 7 Gnd.
A6, 47, 52.	SN7410	TRIPLE 3-INPUT NAND GATES	14 Vcc, 7 Gnd.
A53.	DM7420	DUAL 4-INPUT NAND GATES	14 Vcc, 7 Gnd. 3, 11 NC
A54	SN7404	HEX INVERTERS	14 Vcc, 7 Gnd.
A55.	SN74123	DUAL RETRIGGERABLE MONO MULTIVIBRATOR WITH CLEAR	16 Vcc, 8 Gnd.
A48,49,51.	CTL9956	DUAL 2-INPUT BUFFER	12 Vcc, 5 Gnd., 11 Vee, 3,4,10 n.c
—○		TEST POINTS	

BUREAU OF MINERAL RESOURCES GEOLOGY AND GEOPHYSICS	DRAWING No. X7	SHEET 1	INSTRUMENT 8 CHANNEL D/A CONVERTER X1A-1 SCHEMATIC